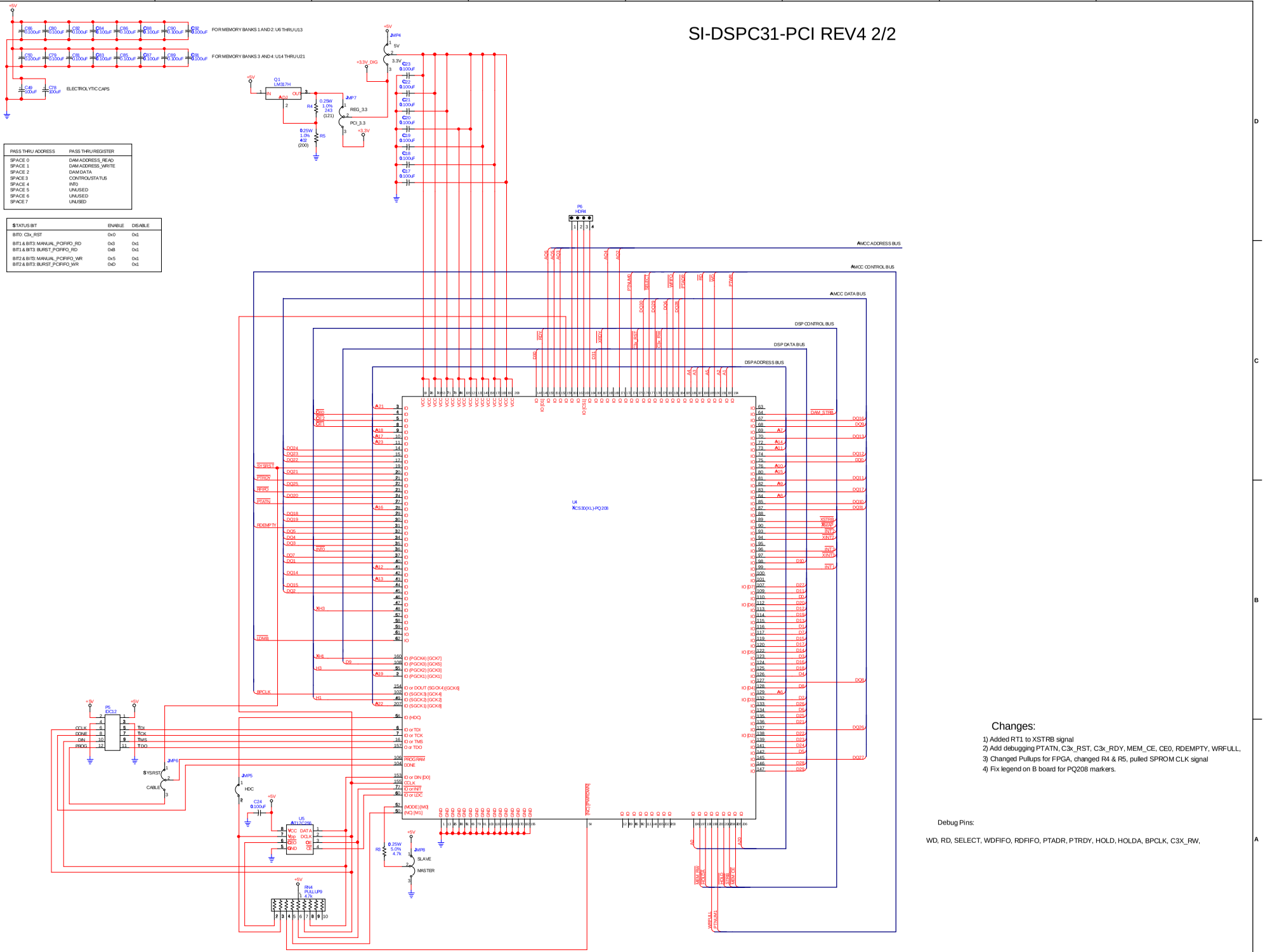
SI-DSPC31-PCI REV4 2/2



PASS THRU ADDRESS	PASS THRU REGISTER
SPACE 0	DAM ADDRESS_READ
SPACE 1	DAM ADDRESS_WRITE
SPACE 2	DAM DATA
SPACE 3	CONTROL/STATUS
SPACE 4	INT0
SPACE 5	UNUSED
SPACE 6	UNUSED
SPACE 7	UNUSED

STATUS BIT	ENABLE	DISABLE
BIT0: C3x_RST	0x0	0x1
BIT1 & BIT3: MANUAL_PCIFIFO_RD	0x3	0x1
BIT1 & BIT3: BURST_PCIFIFO_RD	0xB	0x1
BIT2 & BIT3: MANUAL_PCIFIFO_WR	0x5	0x1
BIT2 & BIT3: BURST_PCIFIFO_WR	0xD	0x1

Changes:

1) Added RT1 to XSTRB signal
2) Add debugging PTATN, C3x_RST, C3x_RDY, MEM_CE, CE0, RDEMPTY, WRFULL,
3) Changed Pullups for FPGA, changed R4 & R5, pulled SPROM CLK signal
4) Fix legend on B board for PQ208 markers.

Debug Pins:

WD, RD, SELECT, WDFIFO, RDFIFO, PTADR, PTRDY, HOLD, HOLDA, BPCLK, C3X_RW,