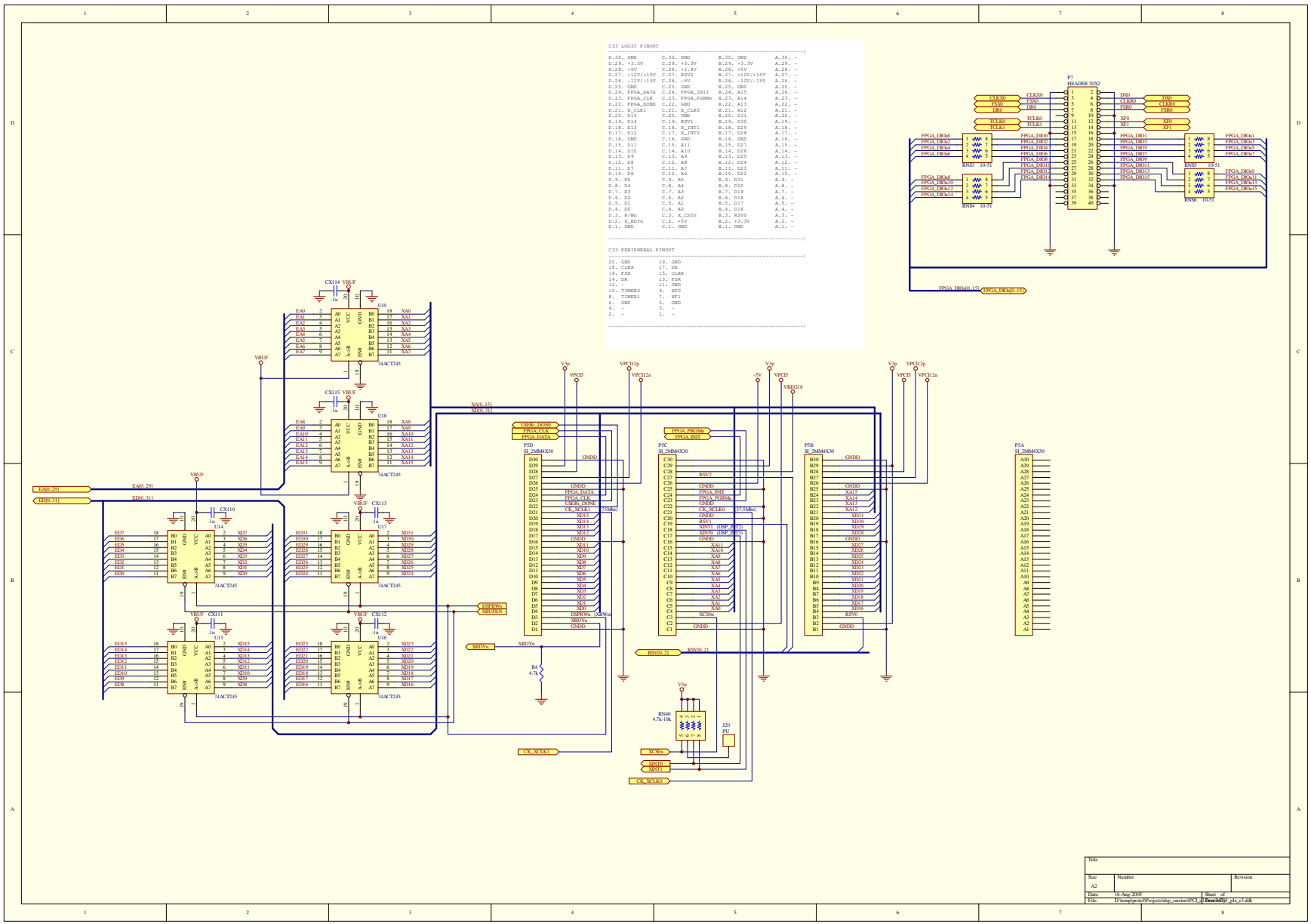
C33 LOGIC PINOUT
C33 PERIPHERAL PINOUT
P7
HEADER 20X2
U19
U18
U17
U16
U15
U14
74ACT245
PSC
PSB
PSA
SL_2MM40X30
PSD
SL_2MM40X30
RN40
4.7k-10k
J20
PJ1
R4
4.7k
FPGA_DIOn[0..15]
EA[0..29]
ED[0..31]
XA[0..15]
XD[0..31]
USERG_DONE
FPGA_CLK
FPGA_DATA
FPGA_PRGMn
FPGA_INIT
DSPRWn
XRDYn
XRSTEN
CK_XCLK1
CK_XCLK0
XC30n
XRSTn
RSV[0..2]
RSV[0..2]
VBUF
V3p
V3n
-5V
VPCI5
VPCI12p
VPCI12n
VREG18
Title
Size
A2
Number
Revision
Date:
16-Aug-2005
Sheet
of
File:
D:\temp\proto2\Projects\dsp_carriers\PCI_C33_dsp_c3.ddb
Drawn By: