HARRIS Semiconductor

DG408, DG409

Single 8-Channel/Differential 4-Channel, CMOS Analog Multiplexers

August 1997

Features

- ON Resistance (25°C Max) 100Ω
- Low Power Consumption (P_D) . . . . . .<11mW
- Fast Switching Action
  - t_{TRANS} . . . . . .<250ns
  - $t_{ON/OFF(EN)}$ . . . . . .<150ns
- Low Charge Injection
- Upgrade from DG508A/DG509A
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Description

The DG408 Single 8-Channel, and DG409 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular DG508A and DG509A series devices. They each include an array of eight analog switches, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

The DG408 and DG409 feature lower signal ON resistance (<100Ω) and faster switch transition time (t_{TRANS} < 250ns) compared to the DG508A or DG509A. Charge injection has been reduced, simplifying sample and hold applications. The improvements in the DG408 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

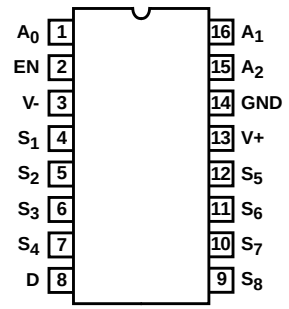
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG408AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG408DJ	-40 to 85	16 Ld PDIP	E16.3
DG408DY	-40 to 85	16 Ld SOIC	M16.15
DG408EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG408EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15
DG409AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG409DJ	-40 to 85	16 Ld PDIP	E16.3
DG409DY	-40 to 85	16 Ld SOIC	M16.15
DG409EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG409EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15

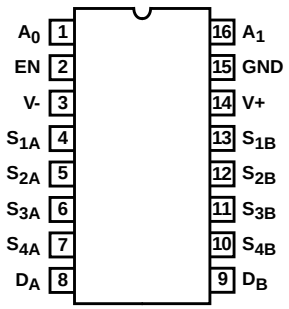
NOTES:
1. Extended Processing Flow
2. Refer to military data sheet for complete specifications.

Pinouts

DG408 (PDIP, CERDIP, SOIC)
TOP VIEW



DG409 (PDIP, CERDIP, SOIC)
TOP VIEW

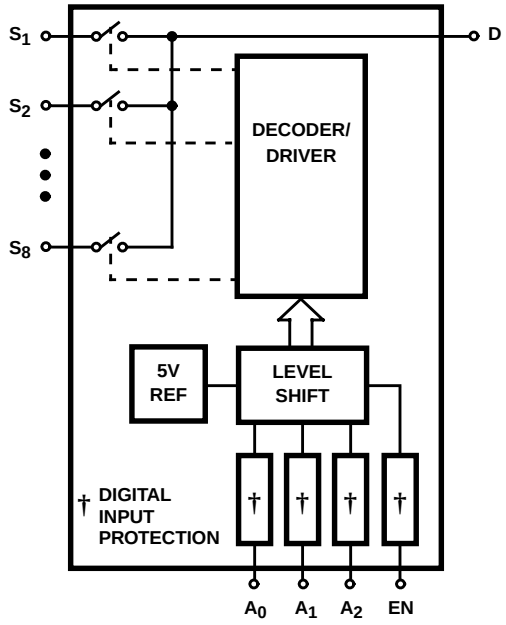


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

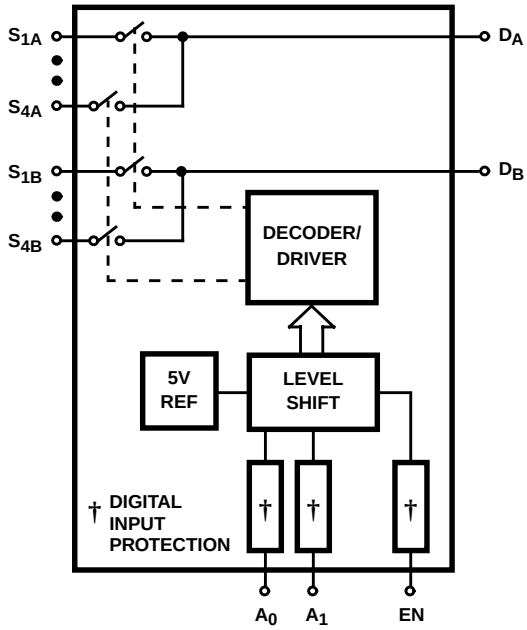
File Number **3283.4**

Functional Block Diagrams

DG408



DG409



Absolute Maximum Ratings

V+ to V- . . . . . +44.0V
GND to V- 25V
Digital Inputs, V_S, V_D (Note 7) . . . . . (V-) -2V to (V+) + 2V or 20mA, Whichever Occurs First
Current (Any Terminal) 30mA
Peak Current, S or D 100mA
(Pulsed 1ms, 10% Duty Cycle)

Operating Conditions

Operating Temperature (D Suffix). . . . . -40C to 85^{o}C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
PDIP Package	100	N/A
SOIC Package	115	N/A
CERDIP Package	70	18

Maximum Junction Temperature (D Suffix) . . . . . 150^{o}C
Maximum Storage Temperature Range (D Suffix) . -65^{o}C to 125^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 8) TEMP	D SUFFIX -40^{o}C TO 85^{o}C (NOTE 2) MIN	(NOTE 3) TYP	(NOTE 2) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 25)	Full	-	160	250	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 27)	Room	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 26)	Room	-	115	150	ns
		Full	-	-	225	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$	(See Figure 26)	Full	-	105	150	ns
Charge Injection, Q	C_L = 10nF, V_S = 0V	Room	-	20	-	pC
OFF Isolation	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 6)	Room	-	-75	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	Room	-	8	-	pF
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	Room	-	3	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$ DG408	V_{EN} = 0V, V_D = 0V, f = 1MHz	Room	-	26	-	pF
DG409		Room	-	14	-	pF
Drain ON Capacitance, $C_{D(ON)}$ DG408	V_{EN} = 3V, V_D = 0V, f = 1MHz, V_A = 0V or 3V	Room	-	37	-	pF
DG409		Room	-	25	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, I_S = -10mA (Note 4)	Room	-	40	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V (Note 5)	Room	-	-	15	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	Room	-0.5	-	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$ DG408	V_{EN} = 0V, V_D = ±10V, V_S = ∓10V	Room	-1	-	1	nA
		Full	-20	-	20	nA
DG409		Room	-1	-	1	nA
		Full	-10	-	10	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 8) TEMP	D SUFFIX -40°C TO 85°C (NOTE 2) MIN	(NOTE 3) TYP	(NOTE 2) MAX	UNITS
Drain ON Leakage Current, $I_{D(ON)}$ DG408	$V_S = V_D = \pm 10V$ Sequence Each Switch ON	Room	-1	-	1	nA
		Full	-20	-	20	nA
DG409		Room	-1	-	1	nA
		Full	-10	-	10	nA
DIGITAL CONTROL						
Logic Input Current, Input Voltage High, I_{AH}	V_A = 2.4V, 15V	Full	-10	-	10	µA
Logic Input Current, Input Voltage Low, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-10	-	10	µA
POWER SUPPLIES						
Positive Supply Current, I+	V_{EN} = 0V, V_A = 0V	Full	-	10	75	µA
Negative Supply Current, I-		Full	-75	1	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V	Room Full	-	0.2	0.5 2	mA
Negative Supply Current, I-		Full	-500	-	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 8) TEMP	D SUFFIX -40°C TO 85°C (NOTE 2) MIN	(NOTE 3) TYP	(NOTE 2) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	Room	-	180	-	ns
Enable Turn-ON Time, $T_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	Room	-	180	-	ns
Enable Turn-OFF Time, $T_{OFF(EN)}$		Room	-	120	-	ns
Charge Injection, Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω	Room	-	5	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 4)	Room	-	90	-	Ω

NOTES:

1. All leads soldered to PC Board.
2. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.
4. Sequence each switch ON.
5. $\Delta r_{DS(ON)} = r_{DS(ON)}$ (Max) - $r_{DS(ON)}$ (Min).
6. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
7. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
8. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

Typical Performance Curves

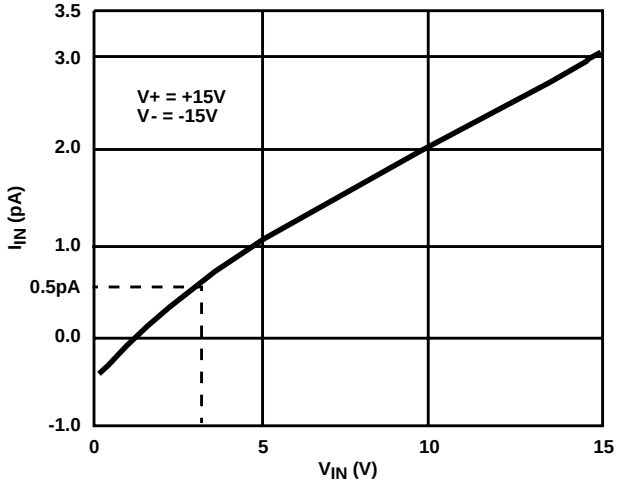


FIGURE 1. INPUT LOGIC CURRENT vs LOGIC INPUT VOLTAGE

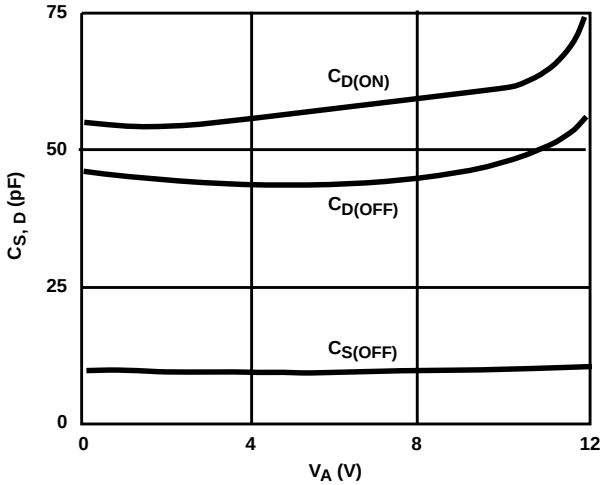


FIGURE 2. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

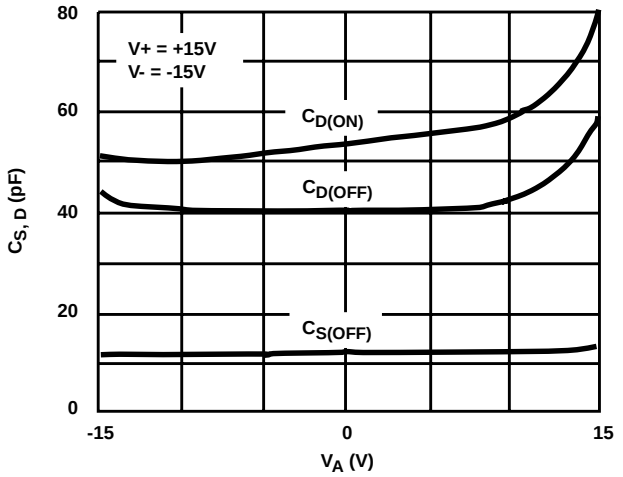


FIGURE 3. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

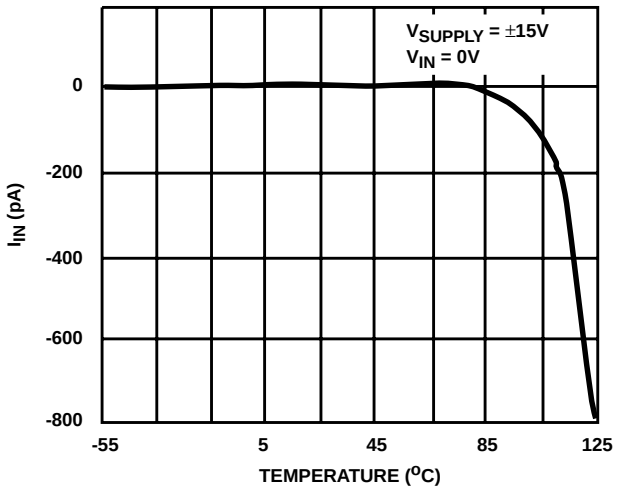


FIGURE 4. LOGIC INPUT CURRENT vs TEMPERATURE

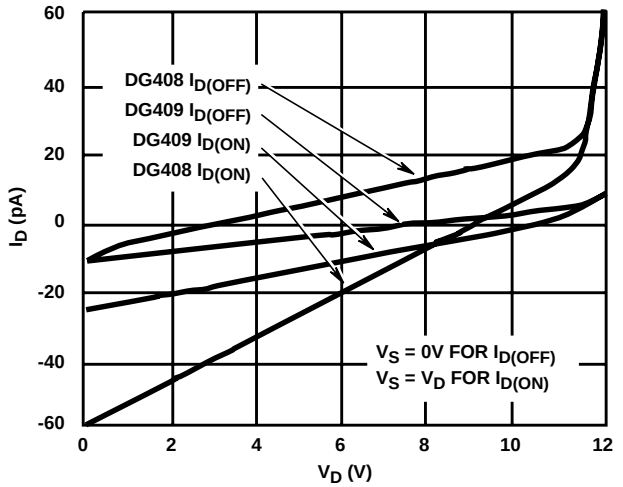


FIGURE 5. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE (SINGLE 12V SUPPLY)

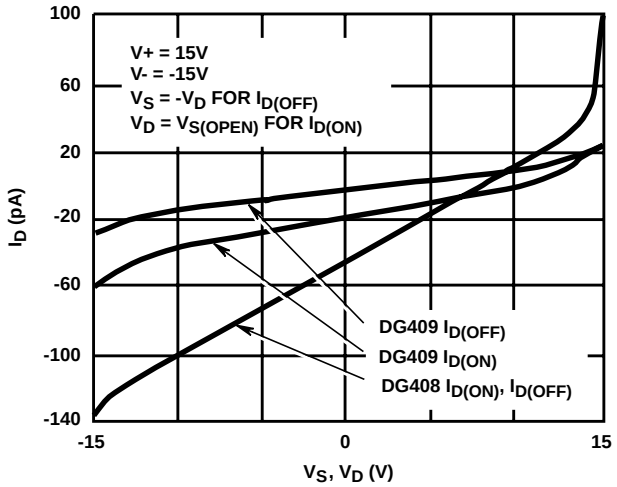


FIGURE 6. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE

Typical Performance Curves (Continued)

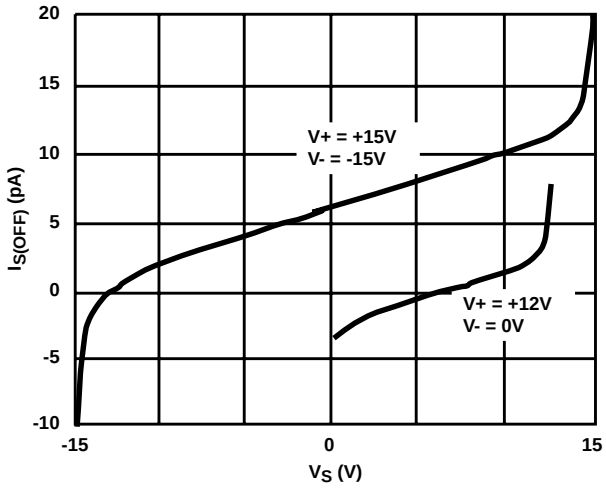


FIGURE 7. SOURCE LEAKAGE CURRENT vs SOURCE VOLTAGE

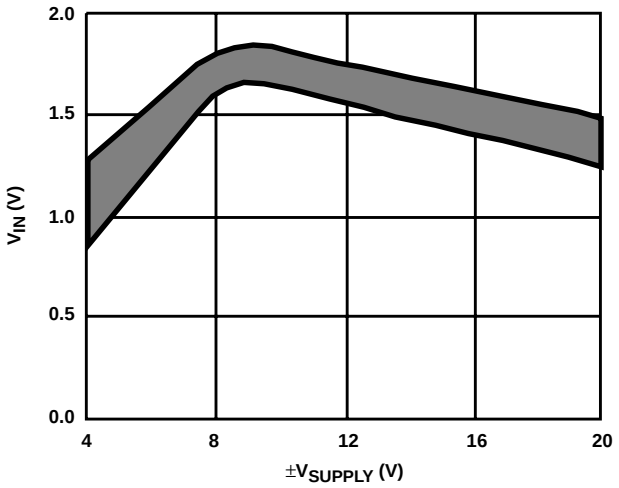


FIGURE 8. INPUT SWITCHING THRESHOLD vs SUPPLY VOLTAGE

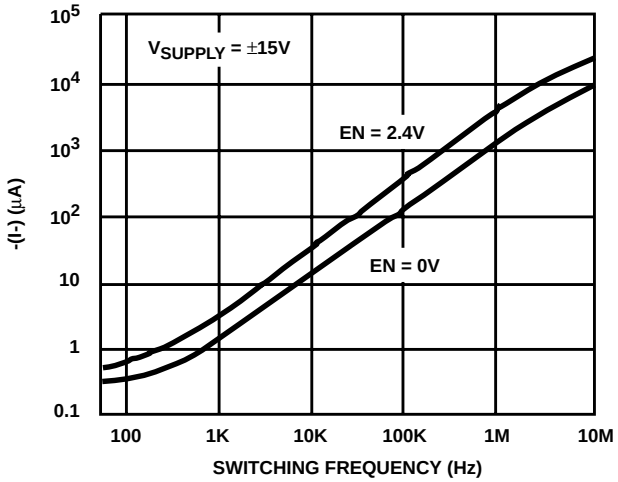


FIGURE 9. NEGATIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

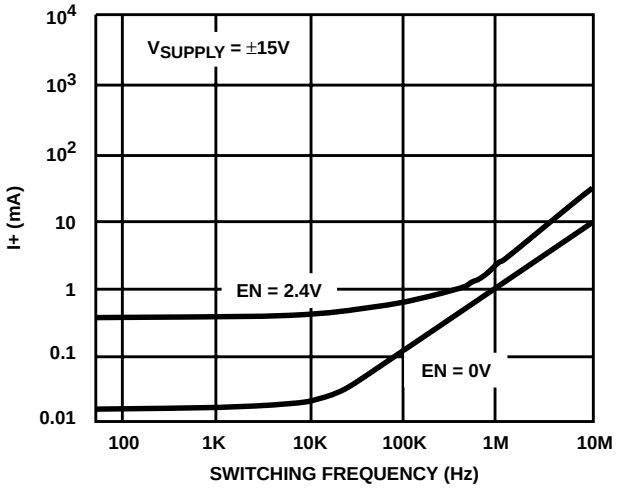


FIGURE 10. POSITIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

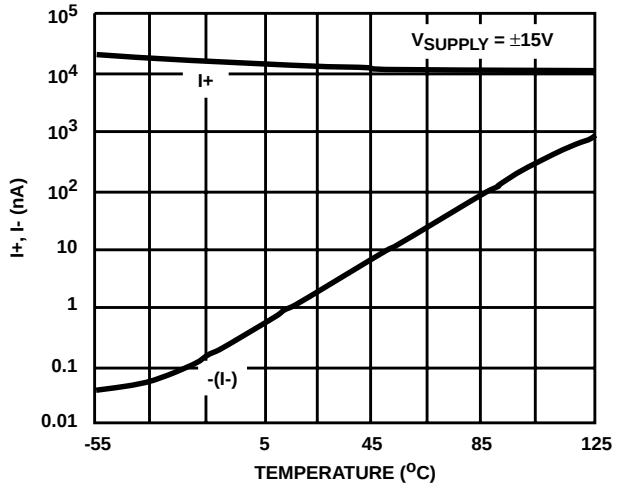


FIGURE 11. I_{SUPPLY} vs TEMPERATURE (LOG SCALE)

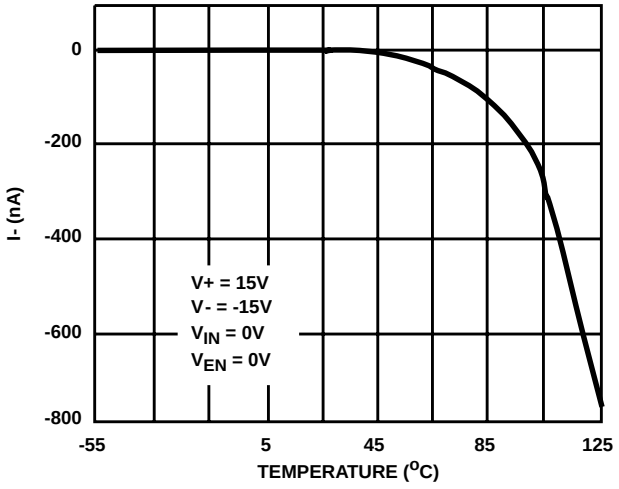


FIGURE 12. NEGATIVE SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

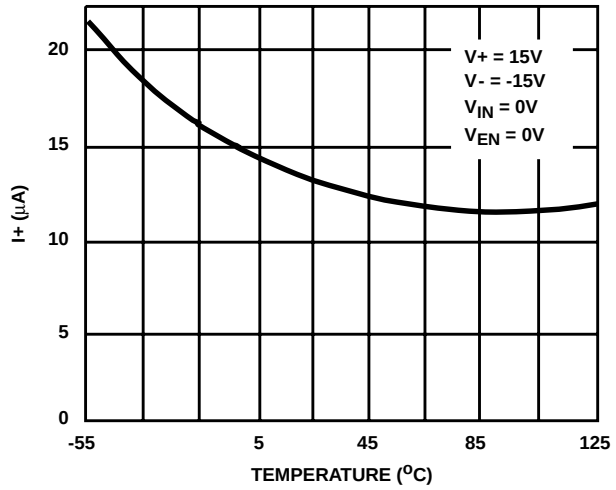


FIGURE 13. POSITIVE SUPPLY CURRENT vs TEMPERATURE (DG408)

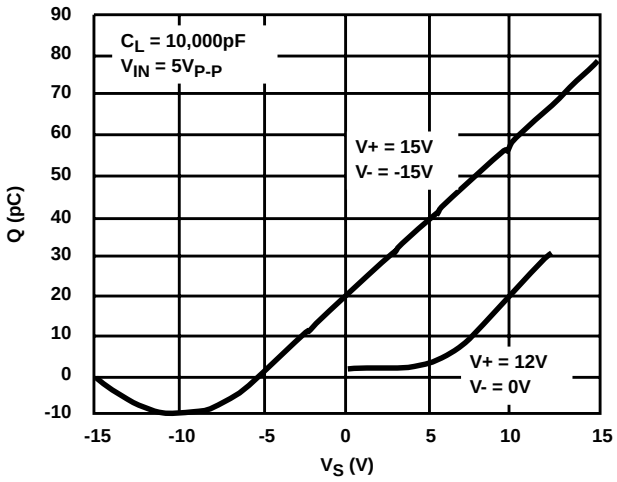


FIGURE 14. CHARGE INJECTION vs ANALOG VOLTAGE V_S (DG408, DG409)

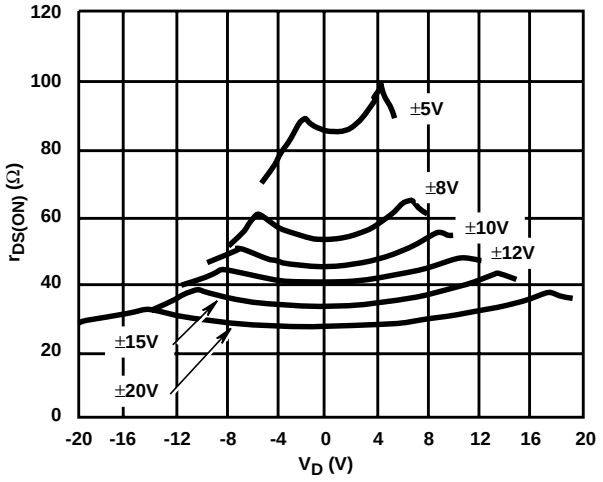


FIGURE 15. $r_{DS(ON)}$ vs V_D AND SUPPLY

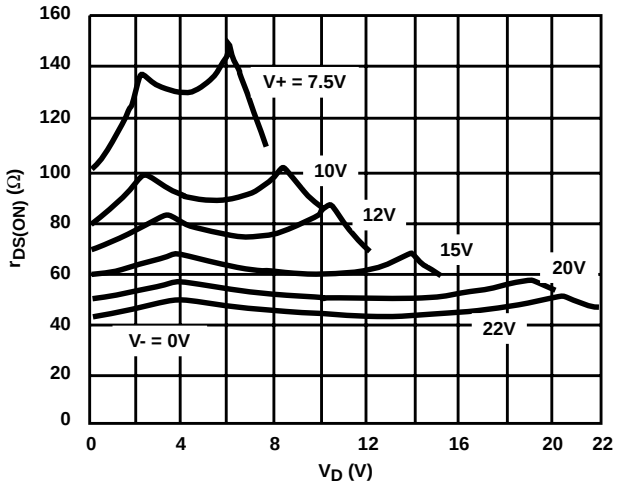


FIGURE 16. $r_{DS(ON)}$ vs V_D (SINGLE SUPPLY)

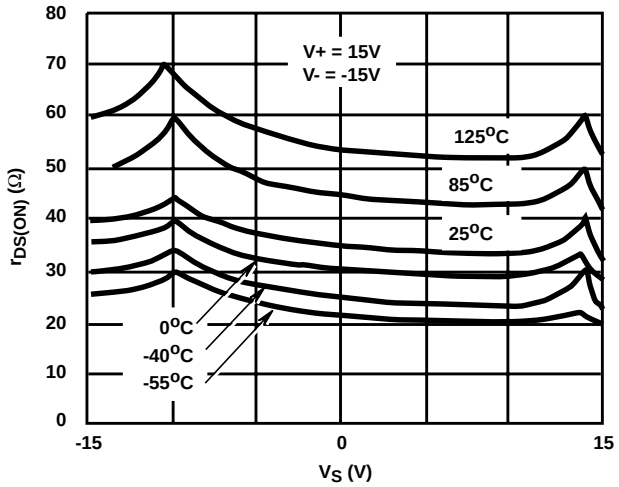


FIGURE 17. $r_{DS(ON)}$ vs V_S AND TEMPERATURE

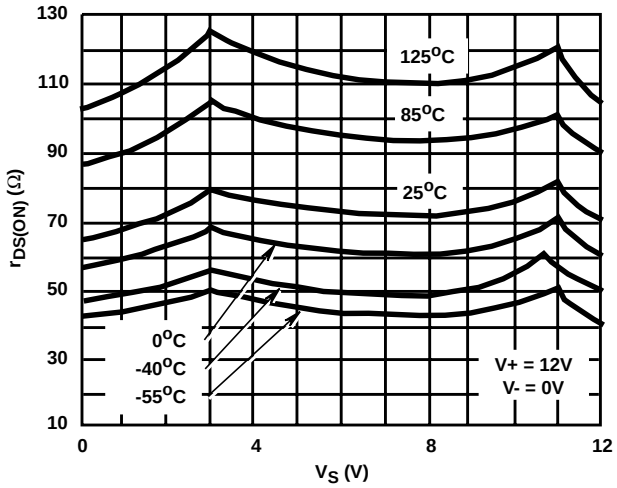


FIGURE 18. $r_{DS(ON)}$ vs V_S AND TEMPERATURE (SINGLE SUPPLY)

Typical Performance Curves (Continued)

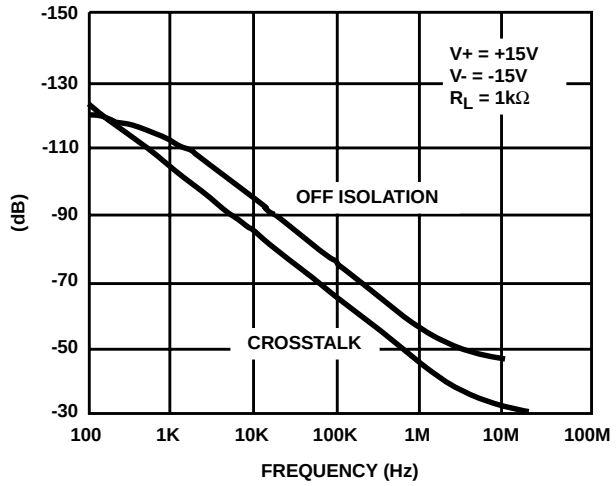


FIGURE 19. OFF ISOLATION AND CROSSTALK vs FREQUENCY

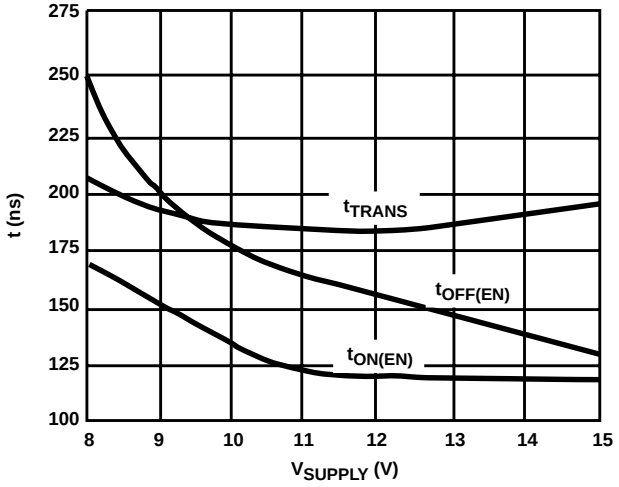


FIGURE 20. SWITCHING TIME vs SINGLE SUPPLY

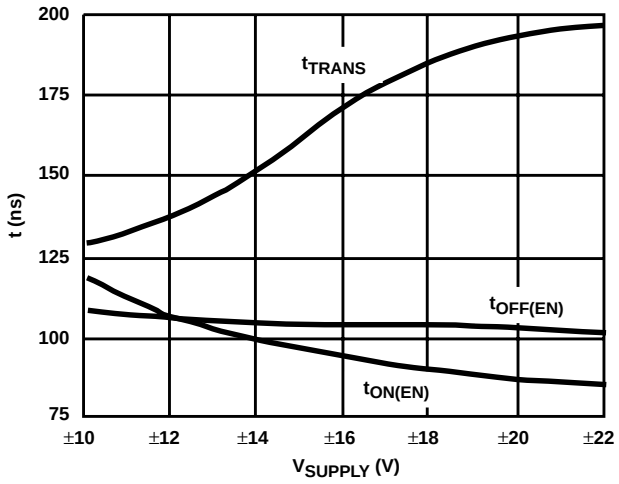


FIGURE 21. SWITCHING TIME vs BIPOLAR SUPPLY

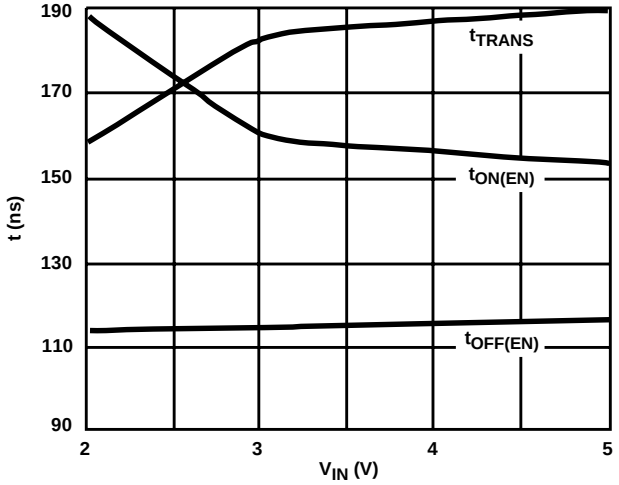


FIGURE 22. SWITCHING TIME vs V_{IN} (SINGLE SUPPLY)

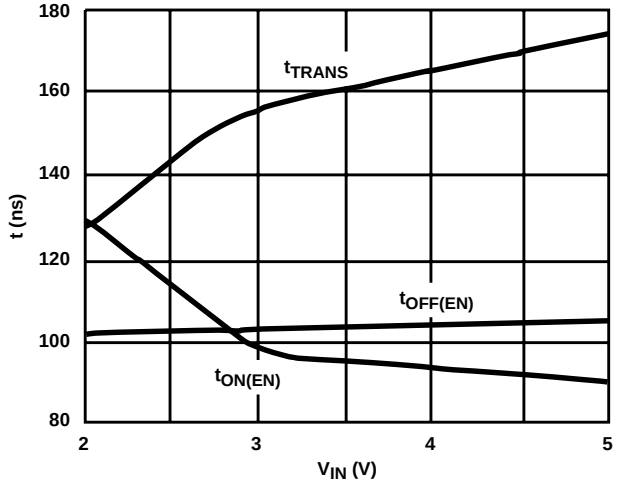


FIGURE 23. SWITCHING TIME vs V_{IN} (BIPOLAR SUPPLY)

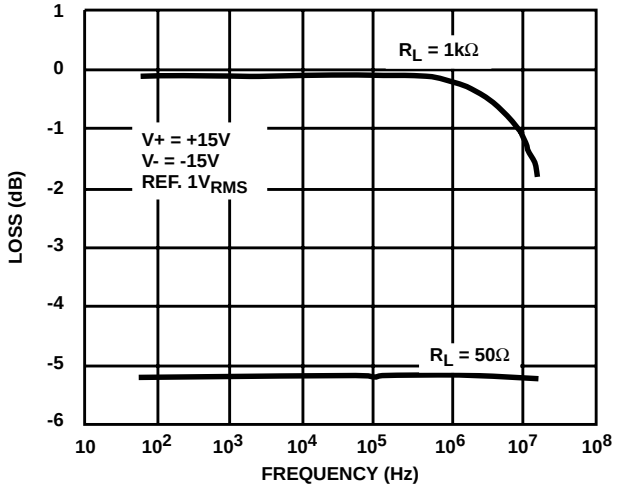


FIGURE 24. INSERTION LOSS vs FREQUENCY

Pin Descriptions - (DG408)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	Negative Power Supply Terminal
4	S_1	Source (Input) for Channel 1
5	S_2	Source (Input) for Channel 2
6	S_3	Source (Input) for Channel 3
7	S_4	Source (Input) for Channel 4
8	D	Drain (Output)
9	S_8	Source (Input) for Channel 8
10	S_7	Source (Input) for Channel 7
11	S_6	Source (Input) for Channel 6
12	S_5	Source (Input) for Channel 5
13	V+	Positive Power Supply Terminal (Substrate)
14	GND	Ground Terminal (Logic Common)
15	A_2	Logic Decode Input (Bit 2, MSB)
16	A_1	Logic Decode Input (Bit 1)

Pin Descriptions - (DG409)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	Negative Power Supply Terminal
4	S_{1A}	Source (Input) for Channel 1a
5	S_{2A}	Source (Input) for Channel 2a
6	S_{3A}	Source (Input) for Channel 3a
7	S_{4A}	Source (Input) for Channel 4a
8	D_A	Drain a (Output a)
9	D_B	Drain b (Output b)
10	S_{4B}	Source (Input) for Channel 4b
11	S_{3B}	Source (Input) for Channel 3b
12	S_{2B}	Source (Input) for Channel 2b
13	S_{1B}	Source (Input) for Channel 1b
14	V+	Positive Power Supply Terminal
15	GND	Ground Terminal (Logic Common)
16	A_1	Logic Decode Input (Bit 1, MSB)

TRUTH TABLE DG408

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG409

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTES:

1. V_{AH} Logic “1” ≥2.4V.
2. V_{AL} Logic “0” ≤0.8V.

Test Circuits and Waveforms

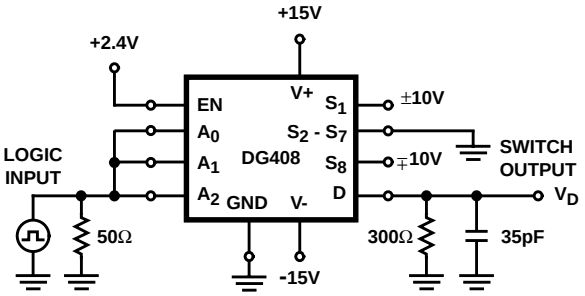


FIGURE 25A.

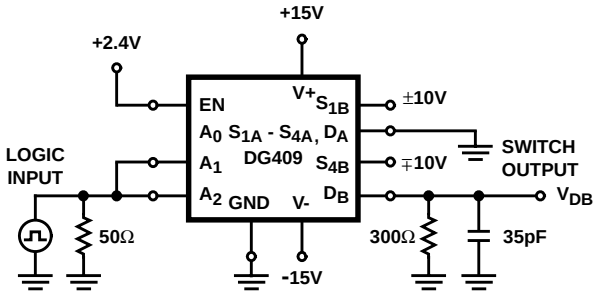


FIGURE 25B.

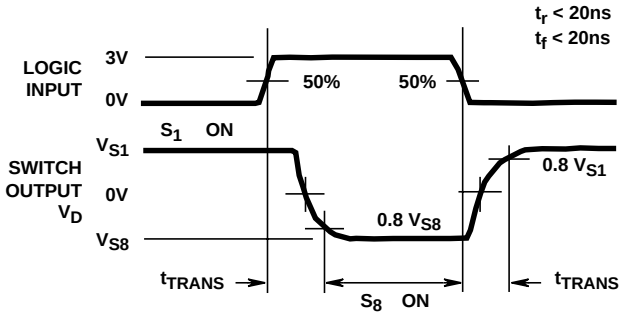


FIGURE 25C.

FIGURE 25. TRANSITION TIME

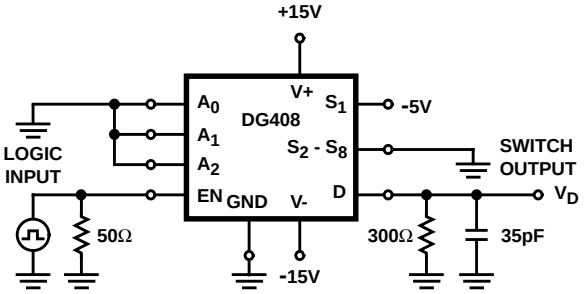


FIGURE 26A.

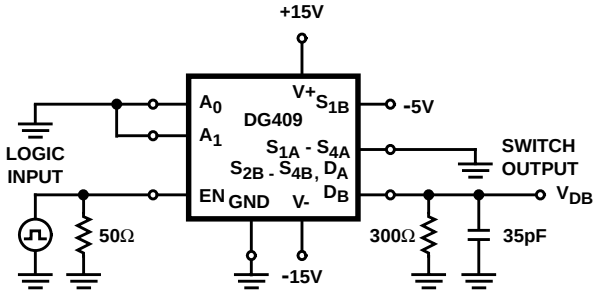


FIGURE 26B.

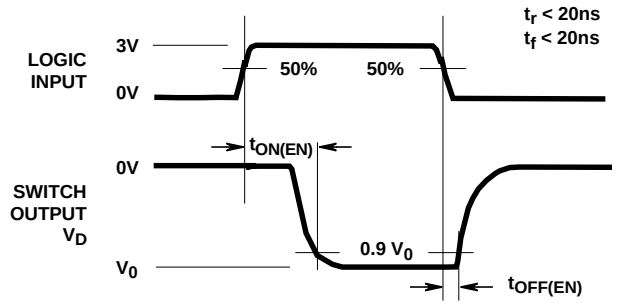


FIGURE 26C.

FIGURE 26. $t_{ON(EN)}$, $t_{OFF(EN)}$

Test Circuits and Waveforms (Continued)

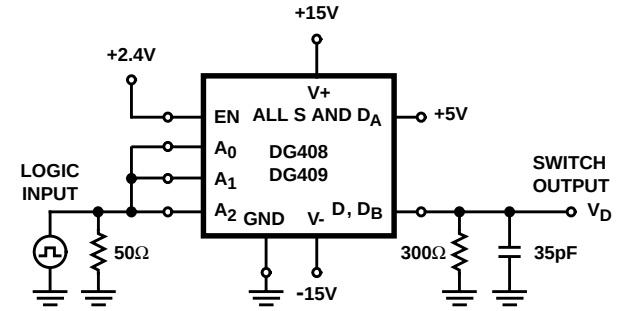


FIGURE 27A.

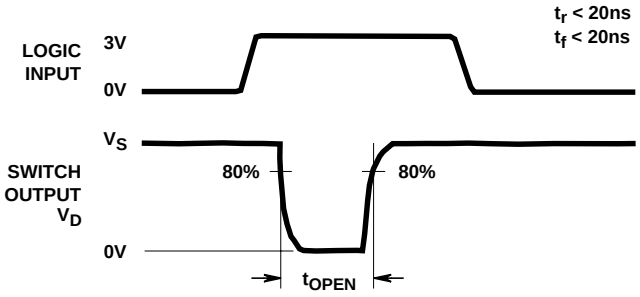


FIGURE 27B.

FIGURE 27. BREAK-BEFORE-MAKE INTERVAL

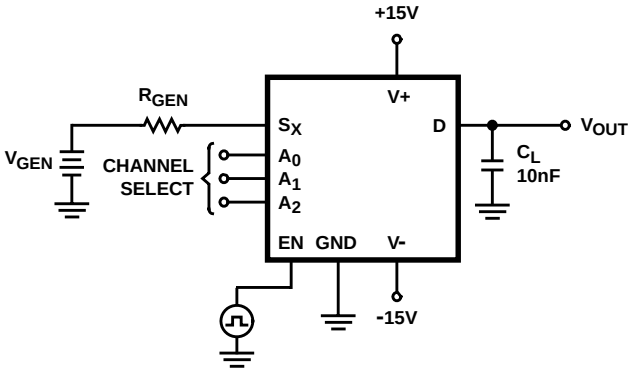
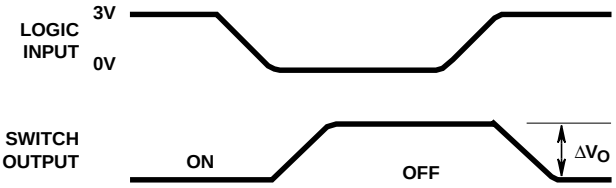


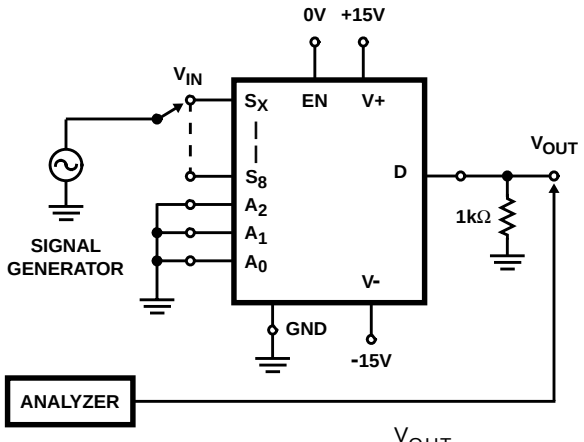
FIGURE 28A.



ΔV_O IS THE MEASURED VOLTAGE DUE TO CHARGE TRANSFER ERROR, Q
$Q = C_L \times \Delta V_O$

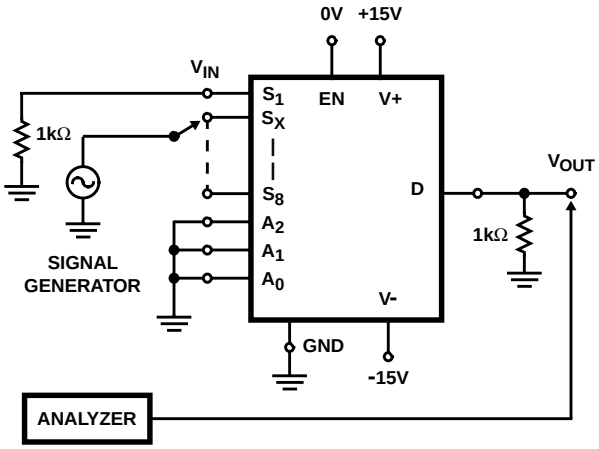
FIGURE 28B.

FIGURE 28. CHARGE INJECTION



$$\text{OFF ISOLATION} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

FIGURE 29. OFF ISOLATION



$$\text{CROSSTALK} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

FIGURE 30. CROSSTALK

Test Circuits and Waveforms (Continued)

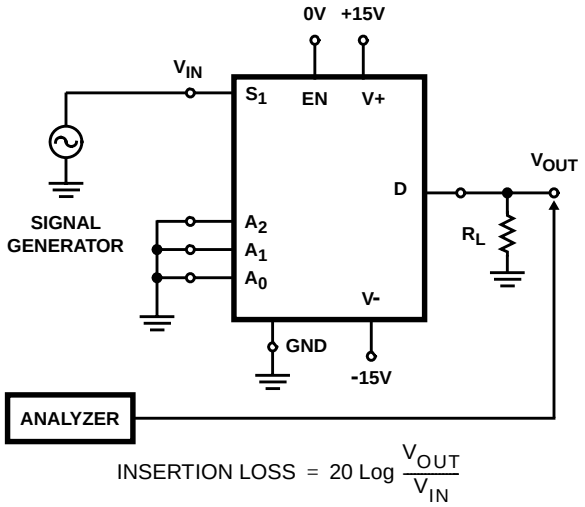


FIGURE 31. INSERTION LOSS

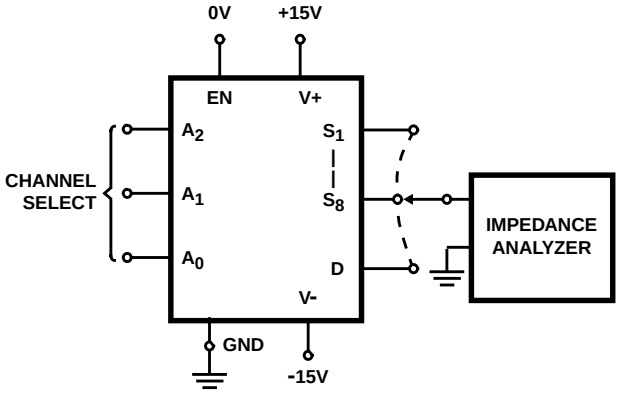


FIGURE 32. SOURCE/DRAIN CAPACITANCES

Typical Applications

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 33). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S - (V-) doesn't exceed -44V. The addition of these diodes will reduce the analog signal range to 1V below V+ and 1V above V-, but it preserves the low channel resistance and low leakage characteristics.

Typical application information is for Design Aid Only, not guaranteed and not subject to production testing.

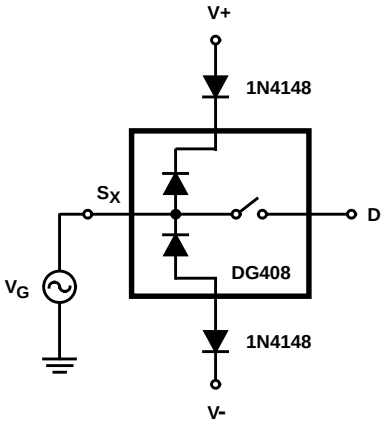


FIGURE 33. OVERVOLTAGE PROTECTION USING BLOCKING DIODES

Die Characteristics

DIE DIMENSIONS:

1800µm x 3320µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

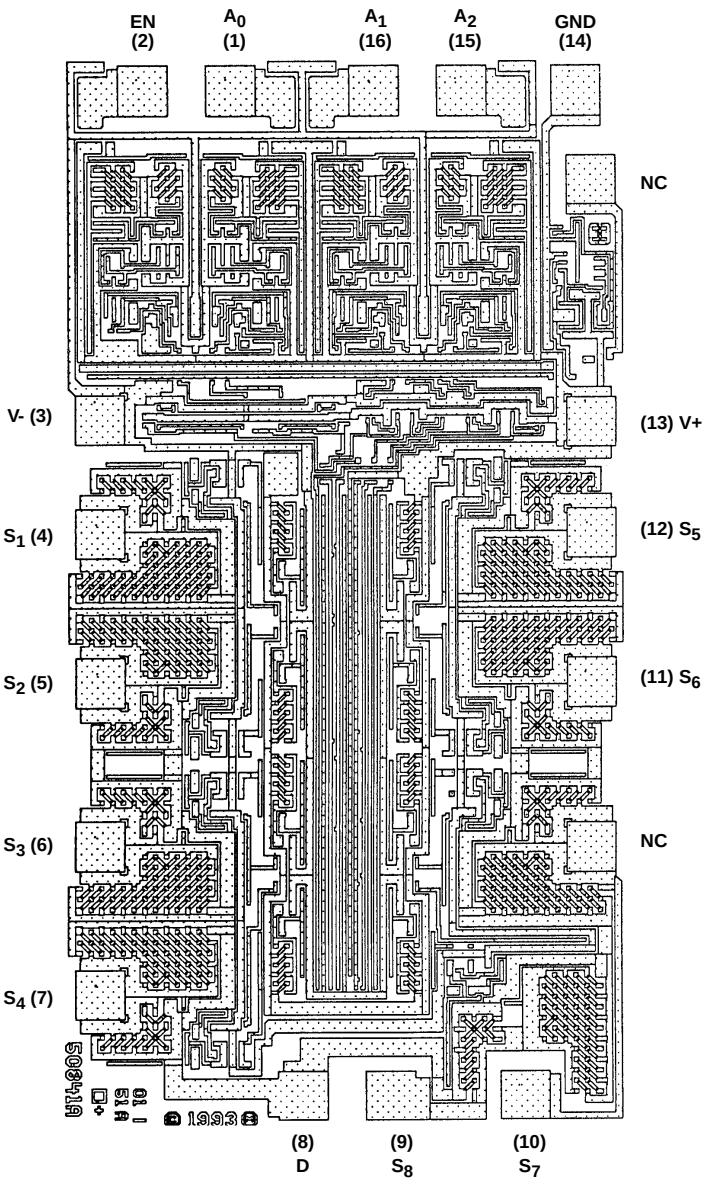
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG408



Die Characteristics

DIE DIMENSIONS:

1800µm x 3320µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG409