SHELDON INSTRUMENTS

SI-DSP1600-PCI User's Guide

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1.0 Introduction

The SI-DSP1600 is a high resolution, multi function data acquisition and control card that plugs into one of the SI-C3XDSP processor cards for either the ISA or PCI busses. A full line of software development tools are available from Sheldon Instruments and TI, which include graphical virtual instrumentation, compilers, assemblers, linkers, as well as a real-time source debugger.

This manual describes the SI-DSP1600 board, its features and design details. Use this manual in conjunction with the SI-C31DSP-PCI/ISA processor card manuals.

1.1 Key Features

- Daughter module to the SI-C31DSP-PCI card and SI-C31DSP-ISA card, forming a DSP based multifunction I/O card.
- 4 independent, simultaneously sampled analog inputs, 16 bit Sigma-Delta ADCs. Complete with 2nd order analog filter and 4096 tap FIR filter to implement a brick wall anti-alias filter front end.
- DDS sample clock generator with ±1hz resolution for a total of 55khz sampling per channel.
- 2 analog outputs, 16 bits resolution, complete with 3rd order smoothing filter.
- Flexible 8 digital I/O.
- Software development tools from Sheldon Instruments, TI; LabVIEW and Hypersignal.
- Windows 3.1x/95/NT support for LabVIEW.
- Easily accessible 15 pin DSUB and 9 pin DSUB connectors.

1.2 Analog Inputs

Each card features 4 analog inputs simultaneously sampled at 16 bits, each with sampling rates ranging from 39hz to 55.8khz with +/-1 hz resolution. The maximum input voltage level is between +/-3Vp, +/-5Vp, or +/-10Vp. The ADCs (Analog Devices AD1878) are based on a Sigma-Delta architecture, which virtually eliminates the need for onboard anti-alias filters. The front end filter consists of a 2nd order analog filter, which complements the ADC's internal 4096 tap FIR filter. Both combine to forma brick wall linear phase filter. Each input can be software configured for AC or DC coupling.

The ADC values are buffered in latches, with the respective channel numbers serving as the latch address offsets to be accessed by the DSP. Every time an entire channel list is digitized, an interrupt (C31's INT3) is generated signaling the DSP that data is ready. In this manner, the DSP simply reads the channels of interest, as it would read any other data on its bus, in a synchronized fashion. The ADC results are stored as a 16 bit, 2's complement signed integer.

1.3 Analog Outputs

Two (2) analog outputs can each update at rates up to 55.8khz, with 16 bits of resolution (Burr-Brown DAC56 or Analog Devices AD1851). These bipolar outputs have a maximum ±10Vp

range, along with a 3-pole linear phase smoothing filter. They are mapped directly on the C31's primary bus. The DAC data is written as a 16 bit, 2's complement signed integer.

1.4 Sample Clock Timer

The sample clock can be derived internally or externally. The onboard sample clock is based on a Direct Digital Synthesizer which provides programmable sampling rates with precision up to ±1hz resolution (Analog Devices AD7008). The DDS is mapped directly on the C31's primary bus. The DDS uses an onboard 50Mhz clock as a reference.

An externally sourced sample clock can also be used to accommodate a variety of sampling schemes. Both of these clocks are also routed to the external two pin jumper connector in the case that multiple cards need to be synchronized to a common clock.

1.5 Digital I/O

8 general purpose digital I/O lines are available, 6 of which can also double as a bi-directional, high speed serial port to the C31 DSP. Please refer to TI's TMS320C3x reference manual for further details.

When configured as digital I/O, each pin's direction can be individually assigned through software.

1.6 Software Support

All functions for the SI-DSP1600 are fully programmable with QuVIEW, which is a library of DSP resident functions that accelerate LabVIEW several times. A full range of examples and tutors are available demonstrating QuVIEW's functionality and capabilities. All QuVIEW drivers fully support Windows 95/NT.

2.0 Register Mapping

All of the DSP1600 components are mapped into the C31's primary bus. These components are initialized to a dormant state upon reset, and must be configured to a desired mode of operation before any tasks are to be performed. Below is a complete summary of registers:

Register	DSP Address (HEX)	Width (Bits)	Direction	Initial Condition
ADC0	0xFE0000	16	Read/Write	Unknown
ADC1	0xFE0001	16	Read/Write	Unknown
ADC2	0xFE0002	16	Read/Write	Unknown
ADC3	0xFE0003	16	Read/Write	Unknown
DAC0	0xFE0100	16	Write only	0 Volts
DAC1	0xFE0101	16	Write only	0 Volts
DDS Reset	0xFE0200	N/A	Write only	Reset
DDS Phase Accumulator, all bytes	0xFE0201	8	Write only	0hz
Start DDS Output	0xFE0202	N/A	Write only	0hz
Control Word	0xFE0203	16	Write only	0x00000000

The DSP1600 configuration must be performed in the following sequence:

1) Write the appropriate operational mode to the Control Register.
2) Write the additive sample rate to the DDS.

3.0 Control Register

The Control Register enables the DDS, DACs, channel coupling modes, analog I/O ranges, and DDS clock source.

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
Control	0xFE0203	16	Write only	0x00000000

3.1 Data Format

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**
CPL3	ATT3	CPL2	ATT2
Bit 11	**Bit 10**	**Bit 9**	**Bit 8**
CPL1	ATT1	CPL0	ATT0
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**
-	-	-	APD
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**
MODE1	MODE0	DAC1-ATTN	DAC0-ATTN

3.2 Control Register Functional Description

Bit Name	Description	Initial Condition
MODE1	Not used	0
MODE0	MODE0= 0 DDS clock is derived from internal 50Mhz clock. MODE0= 1 DDS clock is derived from an external clock.	0
APD	APD = 0 ADCs are on. APD = 1 ADCs are in low power mode or off .	0
DACx-ATTN (DAC0-ATTN thru DAC1-ATTN)	DAC-ATTNx = 0 The maximum output voltage level is ±5V. DAC-ATTNx = 1 The maximum output voltage level is ±10V.	0
CPLx (CPL0 thru CPL3)	CPLx = 0 Input signal is DC coupled. CPLx = 1 Input signal is AC coupled.	0
ATTNx (ATTN0 thru ATTN3)	ATTNx = 0 The maximum input voltage level is ±5V. ATTNx = 1 The maximum input voltage level is ±10V.	0

4.0 DDS Register

The ADC initiates a conversion on the rising edge of the sample clock, divided by a factor of 256. The Sigma-Delta ADCs contain a modulator that convert 64 times the sampling frequency of interest. The ADC sample clock drives all ADCs in parallel according to the followin formula:

ADC Sample Clock = (256) x (Sample Rate per Channel)

Note: *The maximum ADC sample clock value is 55khz for the SI-DSP1600 using Analog Devices' AD1878. Therefore, the DDS can actuallygenerate a maximum of 14.08 Mhz.*

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
DDS Reset	0xFE0201	N/A	Write only	0hz
DDS Phase Accumulator, all bytes	0xFE0201	8	Write only	0hz
Start DDS Output	0xFE0202	N/A	Write only	0hz

The DDS defaults to using a 50Mhz reference clock. The Direct Digital Synthesizer has an internal 32 bit phase accumulator, but only a byte wide interface. Please refer to the Analog Devices AD7008 data sheet for further details. Consequently, it must be accessed in the following specific order:

1) Reset DDS to 0hz. This cycle actually involves toggling the DDS Reset line.
2) Write Phase Accumulator Byte 3, or bits PA31 through PA24.
3) Write Phase Accumulator Byte 2, or bits PA23 through PA16.
4) Write Phase Accumulator Byte 1, or bits PA15 through PA8.
5) Write Phase Accumulator Byte 0, or bits PA7 through PA0.
5) Start the DDS output generation.

5.0 Digital I/O Registers

8 general purpose digital I/O lines are available, 6 of which can also double as a bi-directional, high speed serial port to the C31 DSP. Please refer to TI's TMS320C3x reference manual for further details.

6.0 ADC Registers

The Sigma-Delta ADCs perform simultaneous sampling. The actual requested channel sample rate is derived internally from the ADC by dividing down the supplied DDS clock rate by a factor of 256. The ADC results are latched as 2's complement, 16 bit signed integers, with an interrupt (C31's INT3) signaling the DSP that an entire frame or group of channels has been completed. Each input has a unique memory location that is mapped directly onto the C31's primary bus, with the channel number serving as this memory's address offset.

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
ADC0	0xFE0000	16	Read/Write	Unknown
ADC1	0xFE0001	16	Read/Write	Unknown
ADC2	0xFE0002	16	Read/Write	Unknown
ADC3	0xFE0003	16	Read/Write	Unknown

6.1 Data Format

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
D15 (Sign)	D14	D13	D12	D11	D10	D9	D8
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
D7	D6	D5	D4	D3	D2	D1	D0

7.0 DAC Registers

The DACs are updated by direct C31 writes to its primary bus. Therefore, the only manner in which the DACs may be updated at even intervals is by the DSP servicing interrupts (C31's INT3) caused by the completion of a group of inputs. Please consult the Burr Brown DAC56 (or Analog Devices' AD1851) data sheet for further details.

Note: *The maximum update rate is 55.8khz.*

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
DAC0	0xFE0100	16	Write only	0 Volts
DAC1	0xFE0101	16	Write only	0 Volts

7.1 Data Format

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
D15 (Sign)	D14	D13	D12	D11	D10	D9	D8
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
D7	D6	D5	D4	D3	D2	D1	D0

8.0 Analog I/O Connection for the SI-DSP1600

The 15 pin DSUB plug connector provides the buffered analog signals of the SI-DSP1600 analog I/O module. Their pinouts are as follows:

		1	+INPUT0
AGND0	9		
		2	+INPUT1
AGND1	10		
		3	AGND
AGND2	11		
		4	+INPUT2
AGND3	12		
		5	+INPUT3
AGND	13		
		6	AGND
AGNDOUT0	14		
		7	+OUTPUT0
AGNDOUT1	15		
		8	+OUTPUT1

9.0 Digital I/O Connection for the SI-DSP1600

The 9 pin DSUB socket connector provides the buffered digital signals of the SI-DSP1600 I/O module. Their pinouts are as follows:

		5	XF0
XF1	9		
		4	FSX0
FSR0	8		
		3	DX0
DR0	7		
		2	CLKX0 (port 0)
CLKR0 (port 1)	6		
		1	DGND

10.0 Technical Specifications

10.1 PC interface

- PCI initiated bus master transfer speeds:
  a) Up to 132Mbyte/sec bursts with block sizes of eight (8) 32 bit words.
  b) Up to 20Mbyte/sec sustained transfers of any block size, using the DSP's DMA.

10.2 Analog Inputs

- 4 pseudo differential analog inputs.
- Maximum voltage levels are ±5Vp or ±10Vp.
- High input impedance of 1Mohm.
- Each input has 39hz to 55.8khz simultaneous sampling rate.
- Up to 4 distinct inputs are simultaneously sampled, one from each MUX-PGA-ADC group.
- Onboard DDS for sample rate generator, ±1hz resolution, part # AD7008 (Analog Devices).
- Sigma-Delta ADCs with 16 bits of resolution, part # AD1878 (Analog Devices).
- AC or DC coupling.

10.3 Analog Outputs

- Two (2) DACs for analog output channels, part # DAC56 (Burr Brown) or AD1851 (Analog Devices).
- Each output has 0hz to 55.8khz update rates.
- 16 bits of resolution.
- ±5/±10Vp software selectable bipolar voltage range.
- Fixed 39khz, 3-pole linear phase smoothing filter.

10.4 Digital I/O

- 8 lines individually programmable as inputs or outputs, 6 of which can also double as a bi-directional, high speed serial port to the C31 DSP.

10.5 General features

- Internal and external hardware triggers and sample clocks, software triggers.
- Fully programmable with QuVIEW, an accelerator library for LabVIEW.
- Full suite of development tools from Sheldon Instruments and several third parties.
- Drivers support Win95/NT.

10.6 Physical Dimensions & Electrical Requirements

- SI-DSP1600: 3/4 size PCI-bus card measuring 8.75"(L) x 3.9"(H).
- 9 watts typical.

Appendix A. Analog Devices AD1878

Appendix B. Burr-Brown DAC56

Appendix C. Analog Devices AD7008

Appendix D. National Semiconductor LF347