SHELDON INSTRUMENTS

SI-MOD64xx-PCI User's Guide

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1.0 Introduction

The SI-MOD64xx is a family of high resolution, multifunction data acquisition and control cards that plug into the SI-CxDSP processor card for the PCI bus. A full line of software development tools are available from Sheldon Instruments and TI, which include graphical virtual instrumentation, compilers, assemblers, linkers, as well as a real-time source debugger.

This manual describes the SI-MOD64xx-PCI board, its features and design details. Use this manual in conjunction with the SI-CxDSP-PCI processor card manual.

1.1 Key Features

- Daughter module to the SI-CxDSP-PCI card, forming a DSP based multifunction I/O card.
- 1 to 4 groups of 16 channels, complete with multiplexer, instrumentation amplifier coupled with a programmable gain amplifier, and ADC, for a total of 8DE/16SE, 16DE/32SE, or 32DE/64SE channels of analog inputs, 16 bits resolution.
- Multiple sample clock sources, including optional DDS sample clock generator with ±1hz resolution for a total of 100khz/250khz sampling per MUX-PGA-ADC group.
- 4 analog outputs, 16 bits resolution.
- Flexible 16 digital I/O.
- Software development tools from Sheldon Instruments includes QuVIEW, QuBASE and the SI-DDKs; as well compatibility with TI and third party tools.
- Windows 9x/ME/NT/2000 and Linux support for LabVIEW and Visual Basic.
- Easily accessible 100 pin half pitch DSub (AMP-SCSI style) connector.

1.2 Analog Inputs

Each card features either 8DE/16SE, 16DE/32SE or 32DE/64SE analog input channels. Every group of 8 differential or 16 single ended channels is comprised of its own multiplexer (Harris DG407 and DG409), a two stage programmable gain amplifier (Burr-Brown PGA207 and PGA103) and ADC circuitry (Burr-Brown ADS7805 or Linear Technology LTC1606). Up to four (4) distinct channels, one from each group, can be simultaneously sampled.

The maximum input voltage level is between ±10Vp (or ±8Vp for the high gain or "HG" option), followed by a two stage amplifier that combine to yield gains ranging from 1 to 1,000. The first stage is implemented with a precision differential instrumentation amplifier with gains ranging from 1, 2, 5 and 10 (Burr-Brown PGA207), while the optional second stage is implemented with a precision amplifier with gains of 1, 10, and 100 (Burr-Brown PGA103).

The ADC resolution is 16 bits, each with sampling rates ranging from 0hz to 100khz/250khz, for an additive rate of 400khz/1Mhz respectively, with ±1hz resolution. The ADCs are based on a Successive Approximation architecture, which makes them ideal for control applications (100khz ADC: Burr-Brown ADS7805 or LTC1606; 250khz ADC: Linear Technology LTC1606). Each channel can be individually configured for single or differential ended operation.

The ADC values are buffered in the SRAM, with the respective channel numbers serving as the SRAM address offsets to be accessed by the DSP. Every time an entire channel list is digitized, an interrupt (X_INT0) is generated signaling the DSP that data is ready. In this manner, the DSP simply reads the channels of interest, as it would read any other data on its bus, in a synchronized fashion. The ADC results are stored as a 16 bit, 2's complement signed integer.

1.3 Analog Outputs

Four (4) analog outputs can each update at rates up to 100khz, with 16 bits of resolution (Burr-Brown DAC712). These bipolar outputs have a maximum ±10Vp range, along with a 2-pole linear phase smoothing filter. They are mapped directly on the DSP's primary bus. The DAC data is written as a 16 bit, 2's complement signed integer.

1.4 Sample Clock Timers

The sample clock timer can be derived from one of two onboard circuits or externally, for a total of three possible sources.

The onboard sample clock timers include the choice between 1) a 16 bit counter or 2) an optional onboard Direct Digital Synthesizer (DDS). Both circuits' sample clocks are derived from the same high speed reference clock, and are mapped directly onto the DSP's primary bus.

The first internal sample clock circuit is the classical 'divide by N' implementation of a 16 bit counter. The counter simply increments by integer values on every reference clock transition until a desired, 16 bit preset 'Count' value is reached, at which time a pulse will occur marking the desired sample period.

The second onboard sample clock circuit is based on an optional Direct Digital Synthesizer (DDS), which provides programmable sampling rates with precision up to ±1hz resolution (Analog Devices AD9850).

The third and last source for the sample clock can be user supplied with an external TTL/CMOS level signal, ideal to accommodate a variety of sampling schemes. The external sample clock is taken from the external 100 pin connector.

1.5 Digital I/O

Sixteen (16) general purpose digital I/O lines are available, six (6) of which can also double as a bi-directional, high speed serial port to the DSP. Please refer to TI’s TMS320Cx reference manual for further details.

The other eight (8) lines, labeled as DIOx on the connector, can be configured as a group of inputs or outputs, and are mapped directly on the DSP's primary bus.

1.6 Software Support

All functions for the SI-MOD64xx are fully programmable with QuVIEW and QuBASE, which are a set of DSP-resident libraries for real time performance that greatly accelerate data acquisition, signal processing, and control applications. QuVIEW is a real time accelerator for LabVIEW, and QuBASE a real time accelerator for Visual Basic. A full range of examples and tutors are provided to demonstrate their ease of use and breadth of functionality and capabilities. Complete driver support for Win9x/NT/2000/XP and Linux.

2.0 Register Mapping

All of the SI-MOP64xx components are mapped into the DSP's primary bus. These components are initialized to a dormant state upon reset, and must be configured to a desired mode of operation before any tasks are to be performed. Below is a complete summary of registers:

Register	DSP Address (HEX)	Width (Bits)	Direction	Initial Condition
ADC0 (Inputs 0 thru 15)	0xFE0000 thru 0xFE000F	16	Read/Write	Unknown
ADC1 (Inputs 16 thru 31)	0xFE0010 thru 0xFE001F	16	Read/Write	Unknown
ADC2 (Inputs 32 thru 47)	0xFE0020 thru 0xFE002F	16	Read/Write	Unknown
ADC3 (Inputs 48 thru 63)	0xFE0030 thru 0xFE003F	16	Read/Write	Unknown
DAC0 thru DAC3	0xFE0100 thru 0xFE0103	16	Read/Write	0 Volts
DIO7 thru DIO0	0xFE0200	8	Read/Write	Input Direction
DDS Phase Accumulator, all bytes	0xFE0201	8	Write only	0hz
Start DDS Output	0xFE0202	N/A	Write only	0hz
Control/Status	0xFE0203	16	Read/Write	0x0
16 bit Counter	0xFE0204	16	Write only	0x0
Scan Table/Input Parameters	0xFE0300 thru 0xFE031F	16	Read/Write	Unknown

The SI-MOD64xx configuration must be performed in the following sequence:

1) Write the appropriate operational mode to the Control/Status Register.
2) Download the scan list/mux table and the channel parameter setup to onboard memory.
3) Write the additive sample rate to the sample clock circuits, the counter and the DDS.

3.0 Control/Status Register

The Control/Status Register controls overall board functionality, including the 16 bit counter, the DDS, DACs, and DIOx direction.

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
Control/Status	0xFE0203	16	Read/Write	0x0

3.1 Data Format

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
N/A	N/A	N/A	N/A	N/A	N/A	N/A	CLK_SEL1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DAC3_RES	DAC2_RES	uP_SYS	CLK_SEL0	DIO_DIR	DDS_RES	DAC1_RES	DAC0_RES

3.2 Functional Description

Bit Name	Description	Initial Condition
DAC[3:0]_RES	DACx_RES = 0 Disable DACx output and reset to 0V. Default power up state. DACx_RES = 1 Enable DACx output.	0
DDS_RES	DDS_RES = 0 Enable DDS output. Default power up state. DDS_RES = 1 Disable DDS output, reset to 0hz output.	0
DIO_DIR	DIO_DIR = 0 Configure the 8 DIOx lines as inputs. Default power up state. DIO_DIR = 1 Configure the 8 DIOx lines as outputs.	0
CLK_SEL[1:0]	CLOCK_SEL = 00 ADC additive sample clock sourced from onboard DDS output. SAMPLE_CLK_IO signal (pin 98 on 100 pin Dsub connector) is configured as an output, reflecting the onboard clock signal. Default at power up. CLOCK_SEL = 01 ADC additive sample clock sourced externally from SAMPLE_CLK_IO signal (pin 98 on 100 pin Dsub connector), which is configured as an input. CLOCK_SEL = 10 ADC additive sample clock sourced from onboard 16 bit Counter output. SAMPLE_CLK_IO signal (pin 98 on 100 pin Dsub connector) is configured as an output, reflecting the onboard clock signal. CLOCK_SEL = 11 N/A	0
UP_SYS	uP_SYS = 0 System Data Acquisition mode, disables DSP accesses to the scan/parameters table and ADC data. uP_SYS = 1 uP or microprocessor mode, disables DSP accesses to the scan/parameters table and ADC data.	0

4.0 Clock Sources

The sample clock timer can be derived from one of two onboard circuits or externally, for a total of three possible sources: 1) an onboard 16 bit counter, 2) an optional onboard DDS, and 3) an external source routed through the SAMPL_CLK_IO signal on the 100 pin connector.

4.1 Onboard 16 Bit Counter

The first on board sample clock circuit is the classical 'divide by N' implementation of a 16 bit counter. The 16 bit counter reference clock is derived from the DSP's external clock listed below:

1. SI-C31DSP based cards. For C31 based DSP cards, the 16 bit counter's reference clock uses the C31's Hx clock (half of the DSP's internal clock frequency), which ranges from 20Mhz to 30Mhz.
2. SI-C33DSP based cards. For C33 based DSP cards, the 16 bit counter's reference clock uses half of the C33's Hx clock (one quarter of the DSP's internal clock frequency), which is fixed at 37.5Mhz.
3. SI-C6711DSP based cards. For C6711 based DSP cards, the 16 bit counter's reference clock uses half of the C6711's E clock (one quarter of the DSP's internal clock frequency), which is fixed at 37.5Mhz.

The counter simply increments by integer values on every reference clock transition until a desired, 16 bit preset 'Count' value is reached, at which time a pulse will occur marking the desired, additive sample period. The actual value that is generated by the counter is the additive sample rate of all inputs, based on the following formula:

Additive Sample Clock = (RefClk/(Count + 1)) / Ratio.

The actual value to be downloaded to the counter register is:

Count = (RefClk) / (Additive Sample Clock * Ratio) - 1

where

Additive Sample Clock: Desired sample frequency to ADCs and DACs, derived by multiplying (Number of Channels in the Scan List) x (Sample Rate per Channel).
RefClk: High speed reference clock.
Count: 16 bit preset value loaded to counter register which determines number of RefClk periods to increment.
Ratio: A constant equal to '2'. In order to achieve a perfect 50% duty cycle on both the counter and the DDS outputs, a divide by '2' or toggle flip-flop is used. Therefore, this halving on the onboard circuitry must be compensated in the formula by multiplying the desired additive sampling rate by the same value of '2'.

In other words, the sample rate of each individual channel within a MUX-PGA-ADC section is determined by dividing the Additive Sample Clock rate by the number of channels in the scan list.

For example, if the Additive Sample Clock rate is set to 80khz, and there are a total of 8 channels per MUX-PGA-ADC section defined in the scan list, the each individual channel will be sampling at 10khz.

Note: *The maximum additive sample clock value is 100khz for the SI-MOD64xx-100 boards using Burr Brown's ADS7805 ADC, or 250khz for the SI-MOD64xx-250 boards using Linear Technology's LTC1606. The scan list is limited to a maximum of 16 channels per MUX-PGA-ADC section. Please refer to the Scan List/Input Parameters section for further details.*

Register	DSP Address (HEX)	Width (Bits)	Direction	Initial Condition
16 Bit Count	0xFE0204	16	Write only	0hz

4.2 Onboard DDS

The second on board sample clock circuit is the optional Direct Digital Synthesizer or DDS circuit, which is capable of programmable sampling rates with precision up to ±1hz resolution (Analog Devices AD9850). The DDS reference clock is derived from the DSP's external clock listed below:

1. SI-C31DSP based cards. For C31 based DSP cards, the 16 bit counter's reference clock uses the C31's Hx clock (half of the DSP's internal clock frequency), which ranges from 20Mhz to 30Mhz.
2. SI-C33DSP based cards. For C33 based DSP cards, the 16 bit counter's reference clock uses half of the C33's Hx clock (one quarter of the DSP's internal clock frequency), which is fixed at 37.5Mhz.
3. SI-C6711DSP based cards. For C6711 based DSP cards, the 16 bit counter's reference clock uses half of the C6711's E clock (one quarter of the DSP's internal clock frequency), which is fixed at 37.5Mhz.

Like the onboard counter, the actual value that is generated by the DDS output is the additive sample rate of all inputs, based on the following formula:

Additive Sample Clock = (RefClk * PA) / (Ratio * 2exp32).

The actual value to be downloaded to the DDS phase accumulator (PA) register is:

PA = (Additive Sample Clock * Ratio * 2exp32) / (RefClk)

where

Additive Sample Clock: Desired sample frequency to ADCs and DACs, derived by multiplying (Number of Channels in the Scan List) x (Sample Rate per Channel).
RefClk: High speed reference clock.
PA: 32 bit phase accumulator value loaded to the DDS.

2exp32: A constant reflecting the maximum possible phase accumulator value.
Ratio: A constant equal to '2'. In order to achieve a perfect 50% duty cycle on both the counter and the DDS outputs, a divide by '2' or toggle flip-flop is used. Therefore, this halving on the onboard circuitry must be compensated in the formula by multiplying the desired additive sampling rate by the same value of '2'.

In other words, the sample rate of each individual channel within a MUX-PGA-ADC section is determined by dividing the Additive Sample Clock rate by the number of channels in the scan list.

For example, if the Additive Sample Clock rate is set to 80khz, and there are a total of 8 channels per MUX-PGA-ADC section defined in the scan list, the each individual channel will be sampling at 10khz.

Note: *The maximum additive sample clock value is 100khz for the SI-MOP64xx-100 boards using Burr Brown's ADS7805 ADC, or 250khz for the SI-MOD64xx-250 boards using Linear Technology's LTC1606. The scan list is limited to a maximum of 16 channels per MUX-PGA-ADC section. Please refer to the Scan List/Input Parameters section for further details.*

Register	DSP Address (HEX)	Width (Bits)	Direction	Initial Condition
DDS Phase Accumulator, all bytes	0xFE0201	8	Write only	0hz
Start DDS Output	0xFE0202	N/A	Write only	0hz

The Direct Digital Synthesizer has an internal 32 bit phase accumulator, but only a byte wide interface. Please refer to the Analog Devices AD9850 data sheet for further details. Consequently, it must be accessed in the following specific order:

1) Reset DDS to 0hz. This cycle actually involves toggling the DDS_RES bit of the Control Register HI, followed by a logic LO.
2) Write Phase Accumulator Byte 3, or bits PA31 through PA24.
3) Write Phase Accumulator Byte 2, or bits PA23 through PA16.
4) Write Phase Accumulator Byte 1, or bits PA15 through PA8.
5) Write Phase Accumulator Byte 0, or bits PA7 through PA0.
6) Start the DDS output generation.

The additive sample clock can also be sourced externally by placing a TTL/CMOS level clock on pin 98 of the 100 pin D-sub connector, defined as SAMPLE_CK_IN. Conversely, pin 48 of the 100 pin D-sub connector defined as SAMPLE_CK_OUT, makes the internal/external additive sample clock externally available. This is especially useful if several cards need to be synchronized to a common clock.

4.3 External Sample Clock Source

The sample clock signal may also be supplied by an external TTL/CMOS level source, routed through the SAMPLE_CLK_IO line that resides on pin 98 of the 100 pin DSub connector.

The SAMPLE_CLK_IO line is bi-directional, making it ideal to accommodate a variety of sampling schemes. When the sample clock is selected to be sourced with either the onboard counter or DDS, it is automatically configured as an output. Alternatively, when selected to be sourced externally, it is automatically configured as an input.

5.0 Digital I/O Registers

Sixteen (16) general purpose TTL/CMOS signal level digital I/O lines are available, divided into two groups: 1) eight (8) lines accessible as a single bi-directional byte wide port, and 2) eight (8) lines individually accessible that are routed from the DSP, which can double as either general purpose digital I/O or as a bi-directional, high speed serial port to the DSP. Please refer to TI's TMS320Cx reference manual for further details.

5.1 Digital I/O Byte Wide Port

The eight (8) bi-directional, CMOS/TTL signal level byte wide port lines are labeled as DIOx on the 100 pin connector, and are mapped directly on the DSP's primary bus.

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
DIO7 thru DIO0	0xFE0200	8	Read/Write	Input Direction

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

5.2 Digital I/O Pins From DSP

The eight (8) bi-directional, individual CMOS/TTL signal level lines are labeled on the 100 pin connector as they would function on the DSP when configured as a serial port. By default, they are configured to function as general purpose digital I/O lines, and are mapped within the DSP's configuration registers. Please consult TI's TMS320Cx manual for more details.

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
XF1	FSR0	DR0	CLKR0	XF0	FSX0	DX0	CLKX0

6.0 ADC Registers

The each MUX-PGA-ADC group performs sampling in a time division multiplexed fashion, with the period between each of its samples determined by the additive sample clock. There can be up to four (4) separate MUX-PGA-ADC groups on a single board, giving way to simultaneous sampling on each ADC's input.

The ADC results are stored in memory as a 2's complement 16 bit signed integer, with an interrupt (X_INT0) signaling the DSP that an entire frame or scan of channels has been completed.

Each input has a unique memory location that is mapped directly onto the DSP's primary bus, with the channel number serving as this memory's address offset. In other words, the channel number designation for each MUX-PGA-ADC group always starts with a fixed number, irrespective of the quantity of channels selected for multiplexing or the selected termination style. For example, 'Channel 16' will always refer to the first channel of the second MUX-PGA-ADC group, irrespective of the quantity of channels multiplexed per ADC or its input termination (single or differential ended).

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
ADC0 (Inputs 0 thru 15)	0xFE0000 thru 0xFE000F	16	Read/Write	Unknown
ADC1 (Inputs 16 thru 31)	0xFE0010 thru 0xFE001F	16	Read/Write	Unknown
ADC2 (Inputs 32 thru 47)	0xFE0020 thru 0xFE002F	16	Read/Write	Unknown
ADC3 (Inputs 48 thru 63)	0xFE0030 thru 0xFE003F	16	Read/Write	Unknown

6.1 Data Format

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
D15 (Sign)	D14	D13	D12	D11	D10	D9	D8
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
D7	D6	D5	D4	D3	D2	D1	D0

7.0 DAC Registers

The DACs are updated by direct DSP writes to its primary bus. Therefore, the only manner in which the DACs may be updated at even intervals is by the DSP servicing interrupts (X_INT0) caused by the completion of a scan of inputs. Please consult the Burr Brown DAC712 data sheet for further details.

Note: *The maximum update rate is 100khz.*

Register	**DSP Address (HEX)**	**Width (Bits)**	**Direction**	**Initial Condition**
DAC0	0xFE0100	16	Write only	0 Volts
DAC1	0xFE0101	16	Write only	0 Volts
DAC2	0xFE0102	16	Write only	0 Volts
DAC3	0xFE0103	16	Write only	0 Volts

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
D15 (Sign)	D14	D13	D12	D11	D10	D9	D8
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
D7	D6	D5	D4	D3	D2	D1	D0

8.0 Scan Table/Input Parameter Registers

The Scan Table/Input Parameter list is stored in SRAM that is mapped directly on the DSP's primary bus. A group of channels to be converted is to be defined by setting up a list of channels, along with each channel's signal characteristics before the initiation of a conversion cycle. The list is typically started with the lowest channel number of interest per MUX-PGA-ADC section, all the way to the very last channel of interest. This last channel also has a marker or a SYNC bit that is used to indicate the end of the list, after which the scan table is restarted. Once the entire scan or frame of channels is completed, an X_INT0 is generated to the DSP. At this time, the DSP can simply read from memory the ADC data from one or more of the channels.

Register	DSP Address (HEX)	Width (Bits)	Direction	Initial Condition
Scan Table/Input Parameters	0xFE0300 thru 0xFE031F	16	Read/Write	Unknown

Remember from the DDS section that

Additive Sample Clock = (Number of Channels in the Scan List) x (Sample Rate per Channel).

Note: *The maximum additive sample clock value is 100khz for the SI-MOD64xx-100 boards using Burr Brown's ADS7805 ADC, or 250khz for the SI-MOD64xx-250 boards using Linear Technology's LTC1606. The scan list is limited to a maximum of 16 channels per MUX-PGA-ADC section. Please refer to the Scan List/Input Parameters section for further details.*

The scan list has only 32 locations, 16 even locations and 16 odd locations. Each channel needs a total of two (2) locations in order to define the channel number of interest, along with its corresponding input termination and gain. The actual ordering of the channel numbers is irrelevant, and each channel's input termination can be individually configured for single ended or differential ended operation. In this manner, channels are not thrown away only to keep even channel boundaries on the input muxes. Please consult the Siliconix/Harris DG407 data sheet for further details on the naming convention used for the analog inputs on the 100 pin D-sub connector.

8.1 Data Format - Even Locations

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
MUXB3_1	MUXB3_0	MUXB2_1	MUXB2_0	MUXB1_1	MUXB1_0	MUXB0_1	MUXB0_0
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
N/A	N/A	N/A	N/A	SYNC	MUXA_2	MUXA_1	MUXA_0

MUXB[3..0]_1	**MUXB[3..0]_0**	**MUXB input configuration for all inputs**
0	0	Single ended input INxA
0	1	Differential ended input INxA-INxB
1	0	Single ended input INxB
1	1	Differential ended input INxB-INxA

MUXA_2	**MUXA_1**	**MUXA_0**	**MUXA input configuration, all MUX-PGA-ADC groups**
0	0	0	Enable inputs IN0 (IN1A_x) and IN8 (IN1B_x)
0	0	1	Enable inputs IN1 (IN2A_x) and IN9 (IN2B_x)
0	1	0	Enable inputs IN2 (IN3A_x) and IN10 (IN3B_x)
0	1	1	Enable inputs IN3 (IN4A_x) and IN11 (IN4B_x)
1	0	0	Enable inputs IN4 (IN5A_x) and IN12 (IN5B_x)
1	0	1	Enable inputs IN5 (IN6A_x) and IN13 (IN6B_x)
1	1	0	Enable inputs IN6 (IN7A_x) and IN14 (IN7B_x)
1	1	1	Enable inputs IN7 (IN8A_x) and IN15 (IN8B_x)

Bit Name	Description	Initial Condition
SYNC	SYNC = 0 Continue to the next location in the Scan Table/Input Parameter memory. SYNC = 1 End of frame or scan list. Forces synchronization by starting at the first location in the Scan Table/Input Parameter memory. Additionally, the INT3 interrupt is generated to the DSP indicating that all ADC values pertaining to the last scan/frame are valid.	Unknown

8.2 Data Format - Odd Locations

These bits determine the overall gain by multiplying the gain value of the first stage (PGA207) by the gain value of the second stage (PGA103).

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
PGA3_3	PGA3_2	PGA2_3	PGA2_2	PGA1_3	PGA1_2	PGA0_3	PGA0_2
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PGA3_1	PGA3_0	PGA2_1	PGA2_0	PGA1_1	PGA1_0	PGA0_1	PGA0_0

PGA[3..0]_1	PGA[3..0]_0	PGA207 Differential Amplifier Gains for all MUX-PGA-ADC groups
0	0	1
0	1	2
1	0	5
1	1	10

PGA[3..0]_3	PGA[3..0]_2	PGA103 Amplifier Gains for all MUX-PGA-ADC groups
0	0	1
0	1	10
1	0	100
1	1	N/A

9.0 100 pin D-sub Connection

An AMP 100 pin Series III half pitch, 0.050" DSub connector, manufacturer part 787170-9, is used to interface the external analog and digital I/O signals. Note the I/O signals are marked with binary numbering scheme. For example, the analog inputs start with IN0 for single ended inputs or IN0+ and IN0- for differential ended inputs. Below is their connection diagram.

DB1.1	IN0 / IN0+	DB1.51	IN8 / IN0-
DB1.2	IN1 / IN1+	DB1.52	IN9 / IN1-
DB1.3	IN2 / IN2+	DB1.53	IN10 / IN2-
DB1.4	IN3 / IN3+	DB1.54	IN11 / IN3-
DB1.5	IN4 / IN4+	DB1.55	IN12 / IN4-
DB1.6	IN5 / IN5+	DB1.56	IN13 / IN5-
DB1.7	IN6 / IN6+	DB1.57	IN14 / IN6-
DB1.8	IN7 / IN7+	DB1.58	IN15 / IN7-
DB1.9	AGND	DB1.59	AGND
DB1.10	IN16 / IN16+	DB1.60	IN24 / IN16-
DB1.11	IN17 / IN17+	DB1.61	IN25 / IN17-
DB1.12	IN18 / IN18+	DB1.62	IN26 / IN18-
DB1.13	IN19 / IN19+	DB1.63	IN27 / IN19-
DB1.14	IN20 / IN20+	DB1.64	IN28 / IN20-
DB1.15	IN21 / IN21+	DB1.65	IN29 / IN21-
DB1.16	IN22 / IN22+	DB1.66	IN30 / IN22-
DB1.17	IN23 / IN23+	DB1.67	IN31 / IN23-
DB1.18	AGND	DB1.68	AGND
DB1.19	IN32 / IN32+	DB1.69	IN40 / IN32-
DB1.20	IN33 / IN33+	DB1.70	IN41 / IN33-
DB1.21	IN34 / IN34+	DB1.71	IN42 / IN34-
DB1.22	IN35 / IN35+	DB1.72	IN43 / IN35-
DB1.23	IN36 / IN36+	DB1.73	IN44 / IN36-
DB1.24	IN37 / IN37+	DB1.74	IN45 / IN37-
DB1.25	IN38 / IN38+	DB1.75	IN46 / IN38-
DB1.26	IN39 / IN39+	DB1.76	IN47 / IN39-
DB1.27	AGND	DB1.77	AGND
DB1.28	IN48 / IN48+	DB1.78	IN56 / IN48-
DB1.29	IN49 / IN49+	DB1.79	IN57 / IN49-
DB1.30	IN50 / IN50+	DB1.80	IN58 / IN50-
DB1.31	IN51 / IN51+	DB1.81	IN59 / IN51-
DB1.32	IN52 / IN52+	DB1.82	IN60 / IN52-
DB1.33	IN53 / IN53+	DB1.83	IN61 / IN53-
DB1.34	IN54 / IN54+	DB1.84	IN62 / IN54-
DB1.35	IN55 / IN55+	DB1.85	IN63 / IN55-
DB1.36	AGND	DB1.86	AGND
DB1.37	DACOUT_0	DB1.87	DACOUT_1
DB1.38	DACOUT_2 (AGND)	DB1.88	DACOUT_3 (AGND)
DB1.39	DGND	DB1.89	DGND
DB1.40	DIO_8 / CLKX0	DB1.90	DIO_12 / CLKR0
DB1.41	DIO_9 / DX0	DB1.91	DIO_13 / DR0
DB1.42	DIO_10 / FSX0	DB1.92	DIO_14 / FSR0
DB1.43	DIO_11 / XF0	DB1.93	DIO_15 / XF1
DB1.44	DIO_0	DB1.94	DIO_4
DB1.45	DIO_1	DB1.95	DIO_5
DB1.46	DIO_2	DB1.96	DIO_6
DB1.47	DIO_3	DB1.97	DIO_7
DB1.48	- (SAMPLE_CLK_OUT)	DB1.98	SAMPLE_CLK_IO
DB1.49	DGND	DB1.99	-
DB1.50	+5V	DB1.100	-

10.0 Technical Specifications

10.1 DSP Interface

All board functions tied directly to DSP's primary bus.

10.2 Analog Inputs

- 16S/8D, 32S/16D, or 64S/32D analog inputs, 16:1 MUX part # DG407, 8:2 MUX part # DG409:
  a) SI-MOD6416-100, 16S/8D, 0hz to 100khz additive sampling for all channels.
  b) SI-MOD6432-100, 32S/16D, 0hz to 200khz additive sampling for all channels.
  c) SI-MOD6400-100, 64S/32D, 0hz to 400khz additive sampling for all channels.
  d) SI-MOD6416-250, 16S/8D, 0hz to 250khz additive sampling for all channels.
  e) SI-MOD6432-250, 32S/16D, 0hz to 500khz additive sampling for all channels.
  f) SI-MOD6400-250, 64S/32D, 0hz to 1Mhz additive sampling for all channels.
- ±10Vp maximum input voltage level, or ±8Vp maximum for the "HG" option.
- High input impedance of 1Mohm.
- Two stage amplifiers with gains of 1 to 1,000; first stage with precision differential instrumentation amplifier with gains of 1, 2, 5, 10, part #PGA207 (Burr Brown); second stage with precision amplifier with gains of 1, 10, 100, part #PGA103 (Burr Brown).
- Each MUX-PGA-ADC group has 0hz to 100khz/250khz muxed time division sampling on 16 channels, for a maximum additive rate of 400khz/1Mhz on all channels, respectively.
- Up to 4 distinct inputs are simultaneously sampled, one from each MUX-PGA-ADC group.
- Onboard 16 bit counter or optional DDS for sample rate generator, ±1hz resolution, part # AD9850 (Analog Devices).
- Successive Approximation ADCs with 16 bits of resolution:
  a) 100khz part #ADS7805 (Burr Brown)
  b) 250khz part #LTC1606 (Linear Technology)
- DC coupling.

10.3 Analog Outputs

- Four (4) DACs for analog output channels, part # DAC712 (Burr Brown).
- Each output has 0hz to 100khz update rates.
- 16 bits of resolution.
- ±10Vp bipolar voltage range.
- Fixed 39khz, 2-pole linear phase smoothing filter.

10.4 Digital I/O

- Sixteen (16) lines of general purpose digital lines:

a) Eight (8) lines individually programmable as inputs or outputs, six (6) of which can also double as a bi-directional, high speed serial port to the DSP.

b) Group of eight (8) lines programmable as inputs or outputs.

10.5 General features

- Internal and external hardware triggers and sample clocks, software triggers.
- Fully programmable with QuVIEW, an accelerator library for LabVIEW.
- Fully programmable with QuBASE, an accelerator library for Visual Basic.
- Full suite of development tools from Sheldon Instruments and several third parties.
- Drivers support for Win9x/NT/2000/XP & Linux.

10.6 Physical Dimensions & Electrical Requirements

- SI-MOD64xx: Fits half size DSP-PCI-bus card measuring 6.4"(L) x 3.9"(H).
- 9 watts typical.

Appendix A. Harris DG407

Appendix B. Burr-Brown PGA207 & PGA103

Appendix C. Burr-Brown ADS7805

Appendix D. Linear Technology LTC1606

Appendix E. Burr-Brown DAC712

Appendix F. Analog Devices AD9850