HARRIS Semiconductor

DG406, DG407

Single 16-Channel/Differential 8-Channel, CMOS Analog Multiplexers

August 1997

Features

- **ON-Resistance (Max) 100Ω**
- **Low Power Consumption (P_D) . . . . . <1.2mW**
- **Fast Transition Time (Max) 300ns**
- **Low Charge Injection**
- **TTL, CMOS Compatible**
- **Single or Split Supply Operation**

Applications

- **Battery Operated Systems**
- **Data Acquisition**
- **Medical Instrumentation**
- **Hi-Rel Systems**
- **Communication Systems**
- **Automatic Test Equipment**

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
DG406DJ	-40 to 85	28 Ld PDIP	E28.6
DG406DY	-40 to 85	28 Ld SOIC	M28.3
DG406EJ (Note)	-40 to 85	28 Ld PDIP	E28.6
DG406EY (Note)	-40 to 85	28 Ld SOIC	M28.3
DG406DN	-40 to 85	28 Ld PLCC	N28.45
DG407DJ	-40 to 85	28 Ld PDIP	E28.6
DG407DY	-40 to 85	28 Ld SOIC	M28.3
DG407EJ (Note)	-40 to 85	28 Ld PDIP	E28.6
DG407EY (Note)	-40 to 85	28 Ld SOIC	M28.3
DG407DN	-40 to 85	28 Ld PLCC	N28.45

NOTE: Extended Processing Flow

Description

The DG406 and DG407 monolithic CMOS analog multiplexers are drop-in replacements for the popular DG506A and DG507A series devices. They each include an array of sixteen analog switches, a TTL and CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

These multiplexers feature lower signal ON resistance (<100Ω) and faster transition time (t_{TRANS} < 300ns) compared to the DG506A and DG507A. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG406 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $30V_{P-P}$ signals when operating with ±15V power supplies.

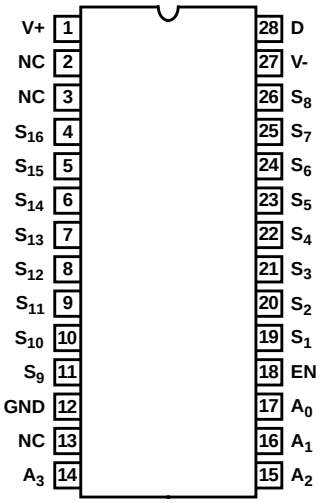
The sixteen switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

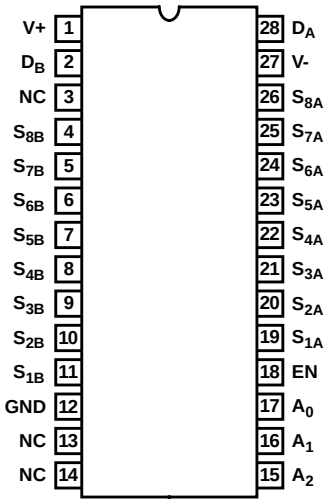
File Number **3116.4**

Pinouts

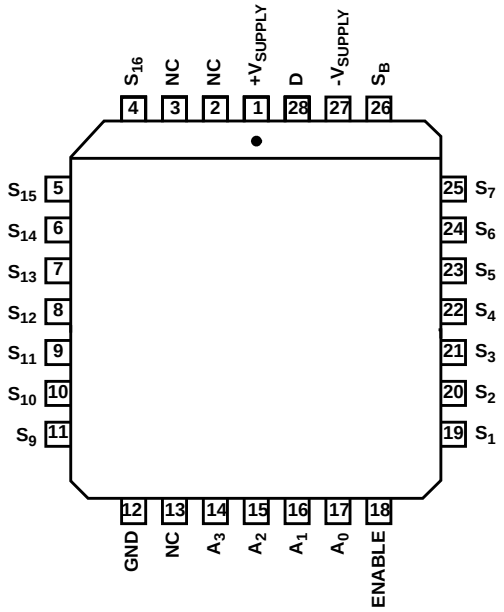
DG406 (PDIP, SOIC)
TOP VIEW



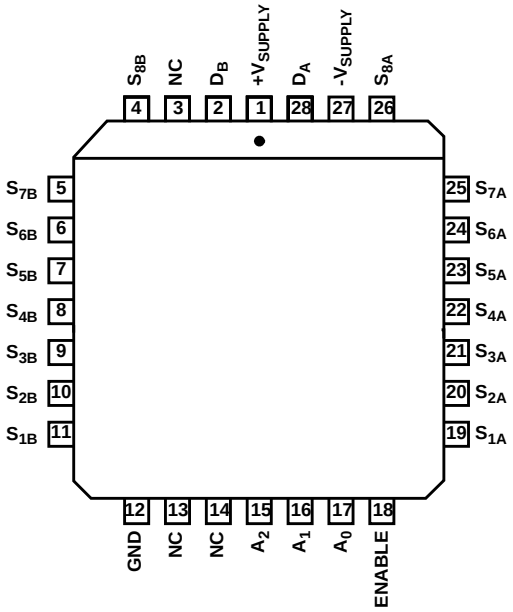
DG407 (PDIP, SOIC)
TOP VIEW



DG406 (PLCC)
TOP VIEW

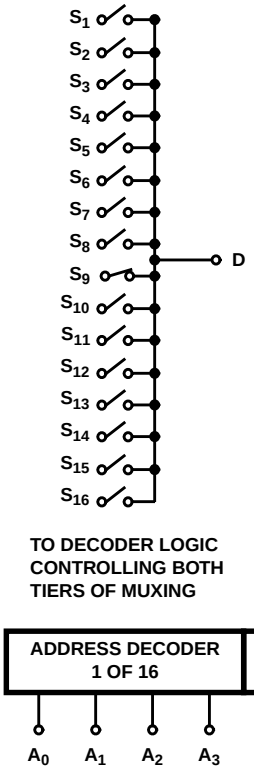


DG407 (PLCC)
TOP VIEW

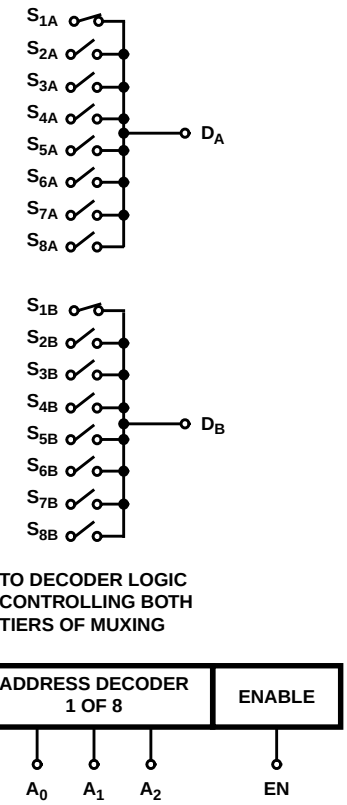


Functional Block Diagrams

DG406



DG407



DG406 TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG407 TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic “0” = V_{AL} < 0.8V
Logic “1” = V_{AH} > 2.4V
X = Don’t Care

Absolute Maximum Ratings

Voltages Referenced to V-
V+ . . . . . +44.0V
GND 25V
Digital Inputs, V_S, V_D (Note 1) . . . . . (V-) -2V to (V+) +2V or 20mA, Whichever Occurs First
Current (Any Terminal) 30mA
Peak Current, S or D 100mA
(Pulsed 1ms, 10% Duty Cycle Max)

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	60
SOIC Package	75
PLCC Package	65

Maximum Junction Temperature . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(PLCC and SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX 40^{o}C TO 85^{o}C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
ANALOG SWITCH						
Drain-Source ON Resistance, $r_{DS(ON)}$	$V_D = \pm 10V$, $I_S = \mp 10mA$ (Note 6)	Room	-	50	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V (Note 7)	Room	-	5	-	%
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, $V_S = \pm 10V$, $V_D = \mp 10V$	Room	-0.5	0.01	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$ DG406		Room	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		Room	-1	0.04	1	nA
		Full	-20	-	20	nA
Drain ON Leakage Current, $I_{D(ON)}$ DG406	$V_S = V_D = \pm 10V$ (Note 6)	Room	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		Room	-1	0.04	1	nA
		Full	-20	-	20	nA
DIGITAL CONTROL						
Logic High Input Voltage, V_{INH}		Full	2.4	-	-	V
Logic Low Input Voltage, V_{INL}		Full	-	-	0.8	V
Logic High Input Current, I_{AH}	V_A = 2.4V, 15V	Full	-1	-	1	µA
Logic Low Input Current, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-1	-	1	µA
Logic Input Capacitance, C_{IN}	f = 1MHz	Room	-	7	-	pF

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX 40°C TO 85°C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 1)	Room	-	200	300	ns
		Full	-	-	400	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 3)	Room	25	50	-	ns
		Full	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 2)	Room	-	150	200	ns
		Full	-	-	400	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		Room	-	70	150	ns
		Full	-	-	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, R_S = 0Ω	Room	-	40	-	pC
OFF Isolation, OIRR	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 8)	Room	-	-69	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	Room	-	8	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$ DG406	V_{EN} = 0V, V_D = 0V, f = 1MHz	Room	-	160	-	pF
DG407		Room	-	80	-	pF
Drain ON Capacitance, $C_{D(ON)}$ DG406	V_{EN} = 5V, V_D = 0V, f = 1MHz	Room	-	180	-	pF
DG407		Room	-	90	-	pF
POWER SUPPLIES						
Positive Supply Current, I+	V_{EN} = V_A = 0V or 5V Stand By	Room	-	13	30	µA
		Full	-	-	75	µA
Negative Supply Current, I-		Room	-1	-0.01	-	µA
		Full	-10	-	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V	Room	-	-0.01	100	µA
		Full	-	-	200	µA
Negative Supply Current, I-		Room	-1	-	-	µA
		Full	-10	-	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX -40°C TO 85°C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	Room	-	300	450	ns

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEMP	D SUFFIX -40°C TO 85°C (NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
Enable Turn-ON Time, $T_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	Room	-	250	600	ns
Enable Turn-OFF Time, $T_{OFF(EN)}$		Room	-	150	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 6V, R_S = 0Ω	Room	-	20	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 6)	Room	-	90	120	Ω
$r_{DS(ON)}$ Matching Between Channels (Note 7), $\Delta r_{DS(ON)}$		Room	-	5	-	%
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_D = 10V or 0.5V, V_S = 0.5V or 10V	Room	-	0.01	-	nA
Drain Off Leakage Current, $I_{D(OFF)}$ DG406		Room	-	0.04	-	nA
DG407		Room	-	0.04	-	nA
Drain On Leakage Current, $I_{D(ON)}$ DG406	$V_S = V_D$ = ±10V (Note 6)	Room	-	0.04	-	nA
DG407		Room	-	0.04	-	nA
POWER SUPPLIES						
Positive Supply Current (I+)	V_{EN} = 0V or 5V, V_A = 0V or 5V	Room	-	13	30	µA
		Full	-	13	75	µA
Negative Supply Current (I-)		Room	-1	-0.01	-	µA
		Full	-5	-0.01	-	µA

NOTES:

3. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
4. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. Typical values are for Design Aid Only, not guaranteed nor production tested.
6. Sequence each switch ON.
7. $\Delta r_{DS(ON)} = r_{DS(ON)}$ (Max) - $r_{DS(ON)}$ (Min) ÷ r_{DS} average
8. Worst case isolation occurs on channel 8B due to proximity to the drain pin.

Test Circuits and Waveforms

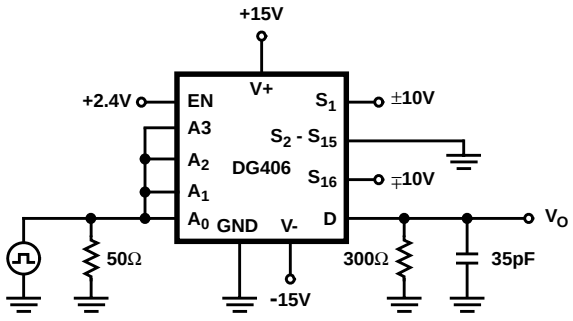


FIGURE 1A.

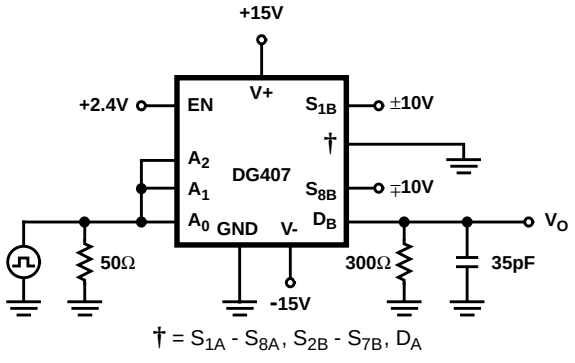


FIGURE 1B.

Test Circuits and Waveforms (Continued)

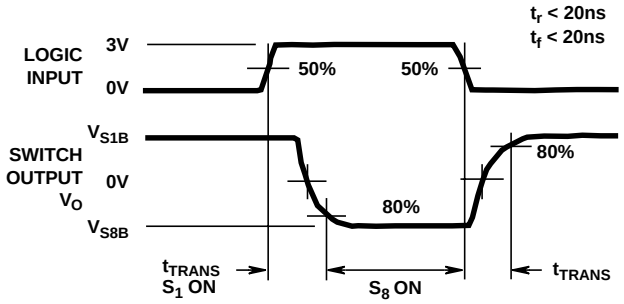


FIGURE 1C.

FIGURE 1. TRANSITION TIME

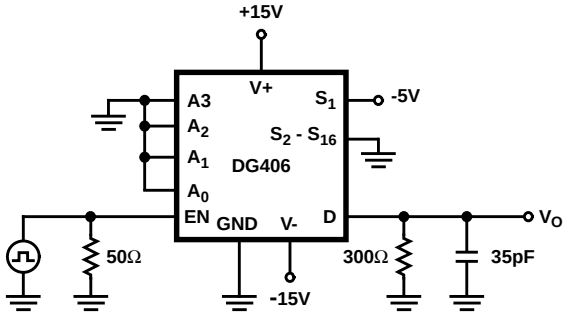


FIGURE 2A.

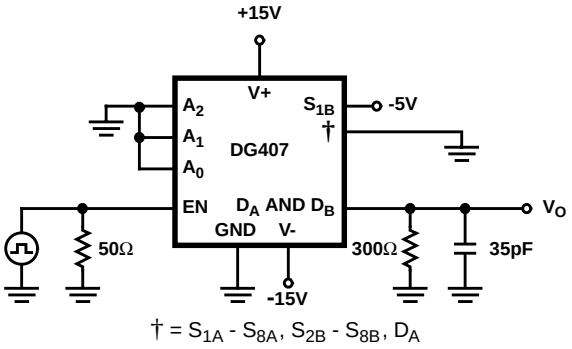


FIGURE 2B.

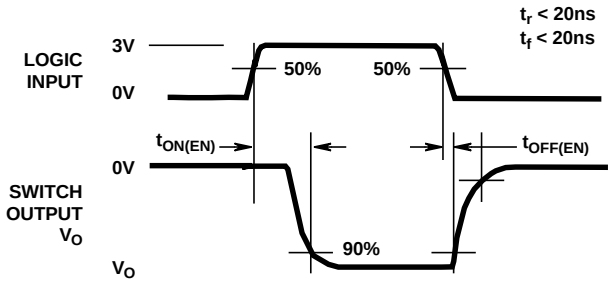


FIGURE 2C.

FIGURE 2. ENABLE SWITCHING TIME

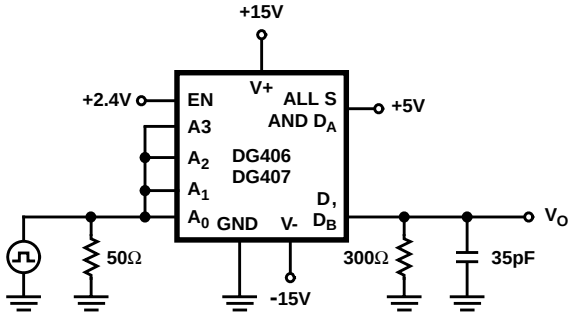


FIGURE 3A.

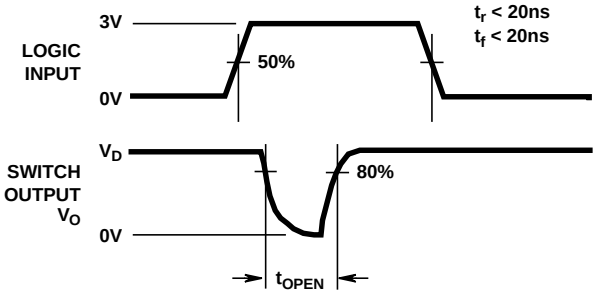


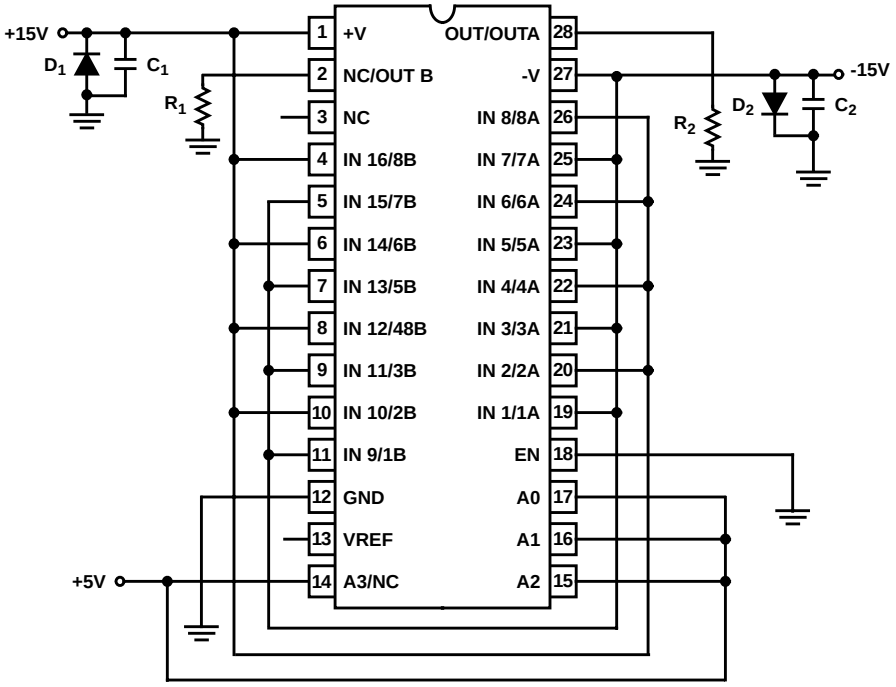
FIGURE 3B.

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL

Burn-In Circuit

CERDIP/SOIC BURN-IN SCHEMATIC

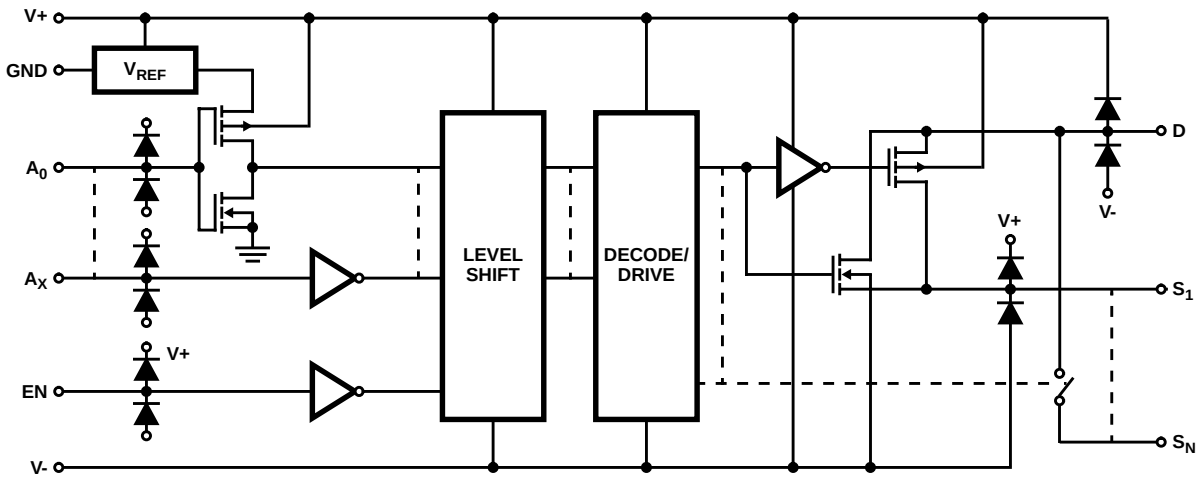
DG406/407EY/EJ



NOTE:

R_1, R_2 = 10kΩ ±5%, $^1/_2$W or $^1/_4$W (Per Socket)
C_1, C_2 = 0.01µF (Min, Per Socket) or 0.1µF (Min, Per Row)
D_1, D_2 = IN402 (or Equivalent, Per Board)

Schematic Diagram (Typical Channel)



Typical Performance Curves

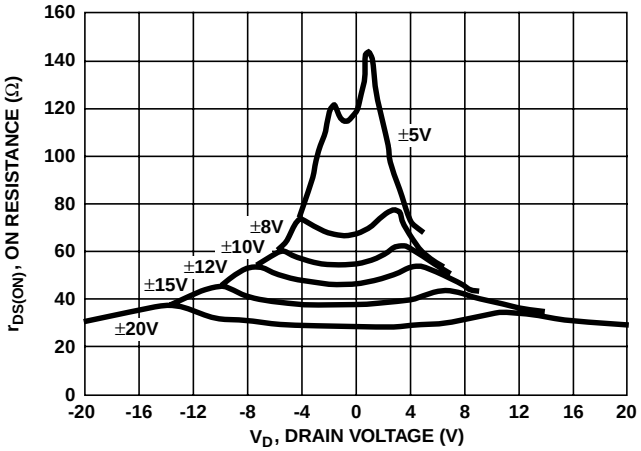


FIGURE 4. $r_{DS(ON)}$ vs V_D AND SUPPLY

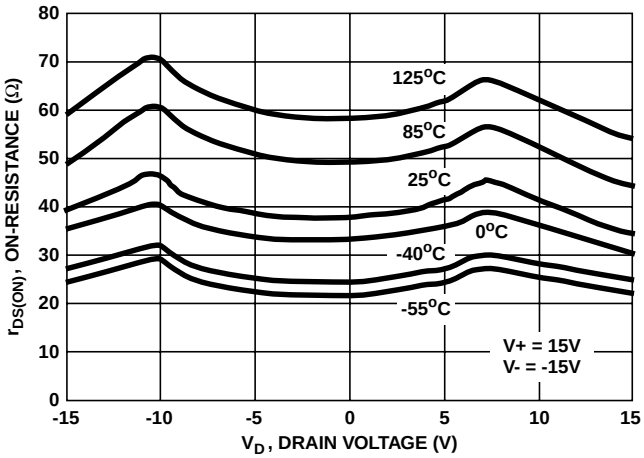


FIGURE 5. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

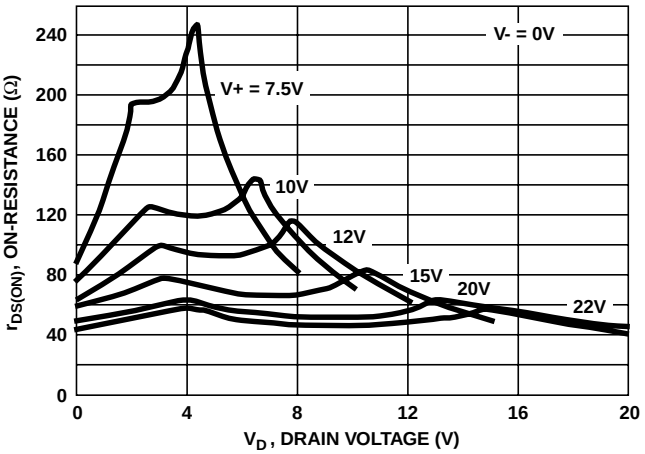


FIGURE 6. $r_{DS(ON)}$ vs V_D AND SUPPLY

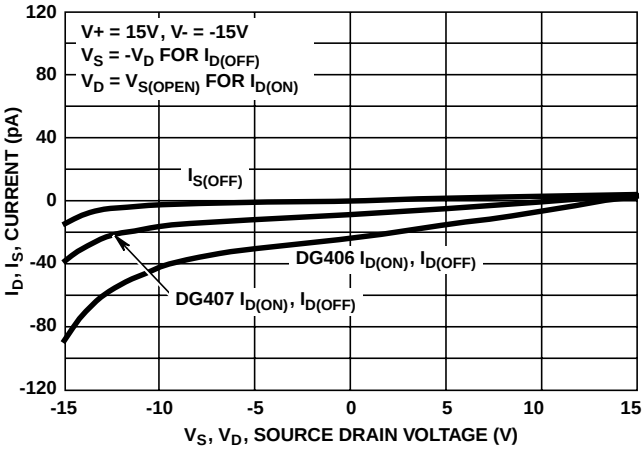


FIGURE 7. I_D, I_S LEAKAGE CURRENTS vs ANALOG VOLTAGE

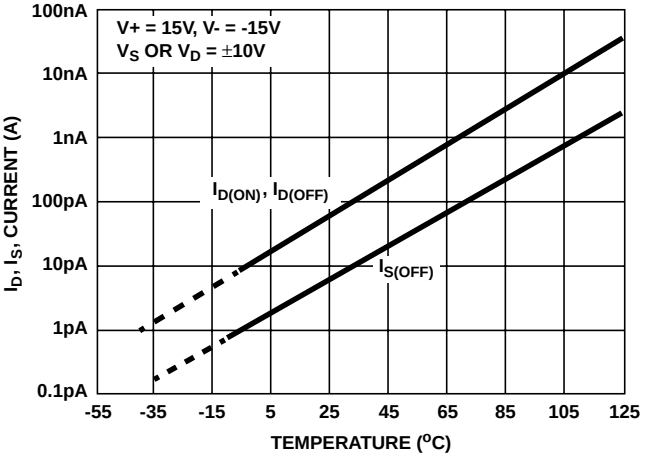


FIGURE 8. I_D, I_S LEAKAGE vs TEMPERATURE

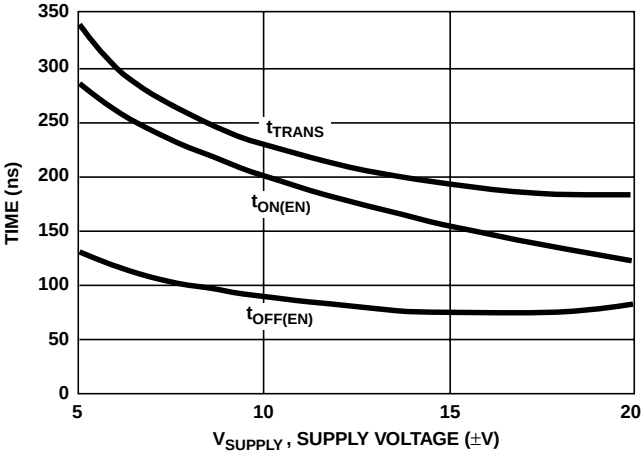


FIGURE 9. SWITCHING TIMES vs BIPOLAR SUPPLIES

Typical Performance Curves (Continued)

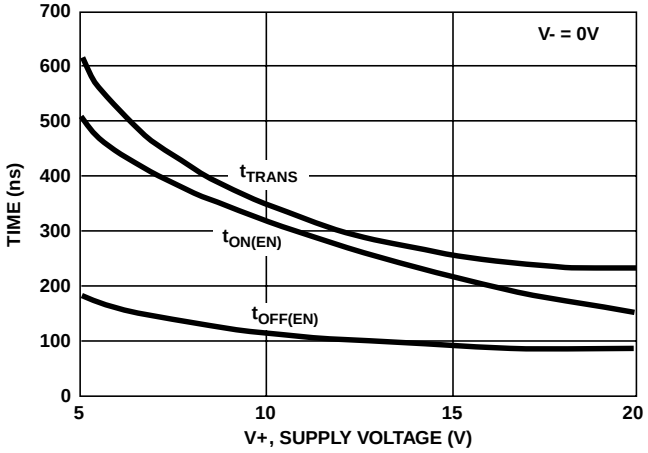


FIGURE 10. SWITCHING TIMES vs SINGLE SUPPLY

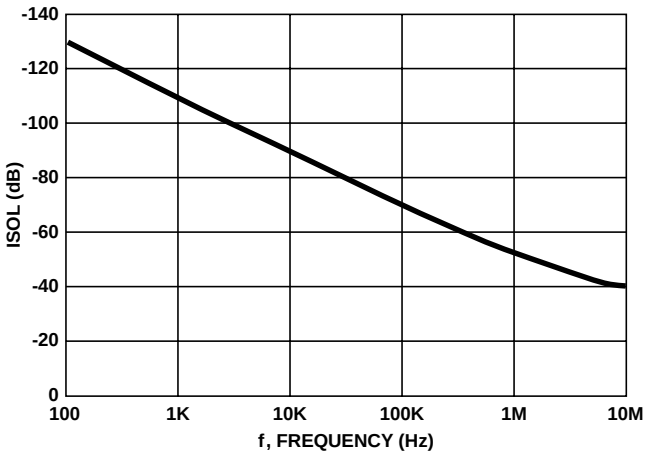


FIGURE 11. OFF-ISOLATION vs FREQUENCY

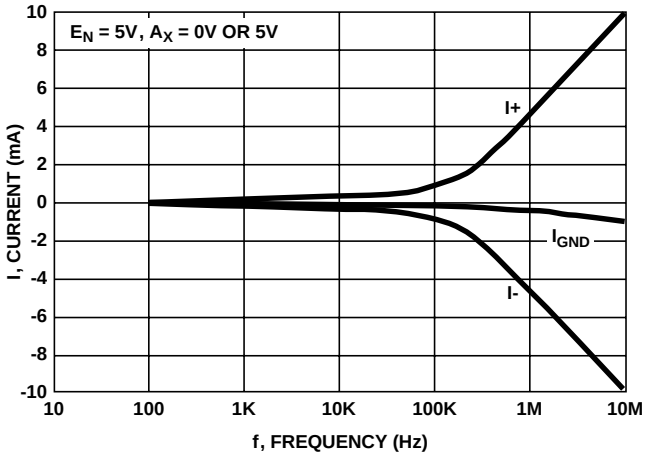


FIGURE 12. SUPPLY CURRENTS vs SWITCHING FREQUENCY

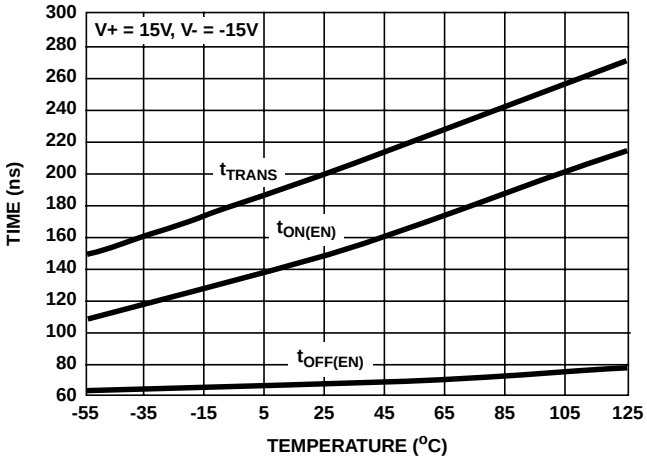


FIGURE 13. t_{ON}/t_{OFF} vs TEMPERATURE

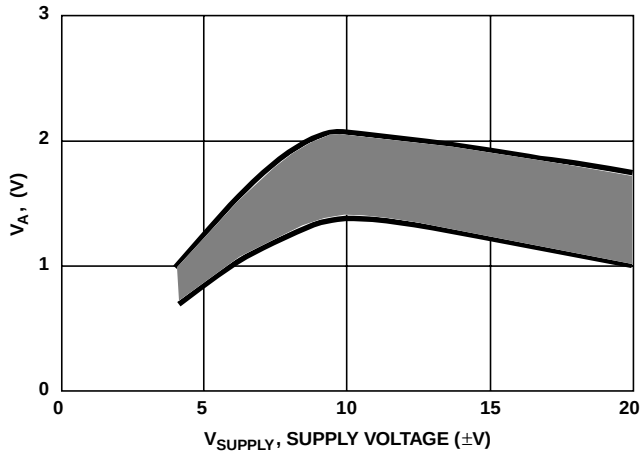


FIGURE 14. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

2490µm x 4560µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

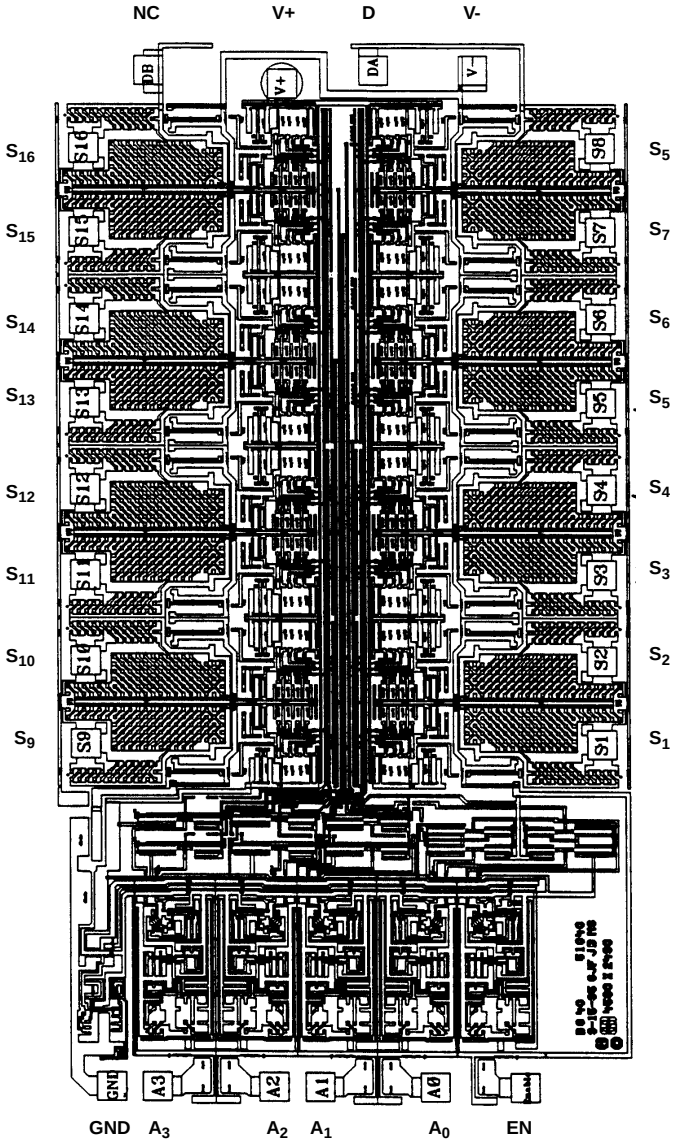
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG406



Die Characteristics

DIE DIMENSIONS:

2490µm x 4560µm x 485µm ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG407